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An 8-bit, 3v, bicmos, video rate analog-to-digital converter design

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AN 8-BIT, 3V, BICMOS, VIDEO RATE ANALOG-TO-DIGITAL CONVERTER DESIGN

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ABSTRACT

AN 8-BIT, 3V, BICMOS, VIDEO RATE
ANALOG-TO-DIGITAL CONVERTER DESIGN

by Edgardo A. Laber

This thesis discusses the design of an Integrated 8-bit Analog-to-Digital Converter. The design is done in a technology which includes a 4GHz NPN Bipolar transistor, and both P and N type MOSFET transistors with 2μm minimum feature size, and with -.3V and +.3V threshold voltages.

The circuit achieves a conversion rate of 18Msamples/sec with a 3.3±.3V power supply, and a 2Vp-p input signal.

This is a "flash" converter that employs a fully differential architecture for both the input buffer and the comparators.

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CHAPTER 1

Analog-to-Digital Converter Background

The purpose of this first chapter is to discuss the need for analog-digital interfaces, and to describe different analog-to-digital (A/D) converter architectures along with their advantages and disadvantages.

Currently, there is a tendency to shift as many functions as possible from the analog to the digital world. In this way integrated circuits become more reliable, are faster to design, easier to program, and it is simpler to interface with digital systems which only understand the language of ones and zeros. Nevertheless, analog circuitry is sometimes a better solution for many design situations. In particular, it is suitable for very high frequency, and when an interaction with analog signals is required. This points out a key fact: While digital circuits work with discrete quantities, those in the real world are continuous. To overcome this barrier, and to be able to use digital technology in dealing with analog quantities, there arises the need for converters. Without them, the amazing advances of modern technology would not have become so common to our lives (fig. 1).

The translation between domains is actually done by A/D and D/A interfaces. They basically convert a certain range of a continuous variable to a level of a discrete variable. The process is called quantization and its resolution depends on how many binary digits (bits) form each discrete value. Fig. 2 shows a 3 bits quantizer transfer function and the result of quantizing a sine wave.

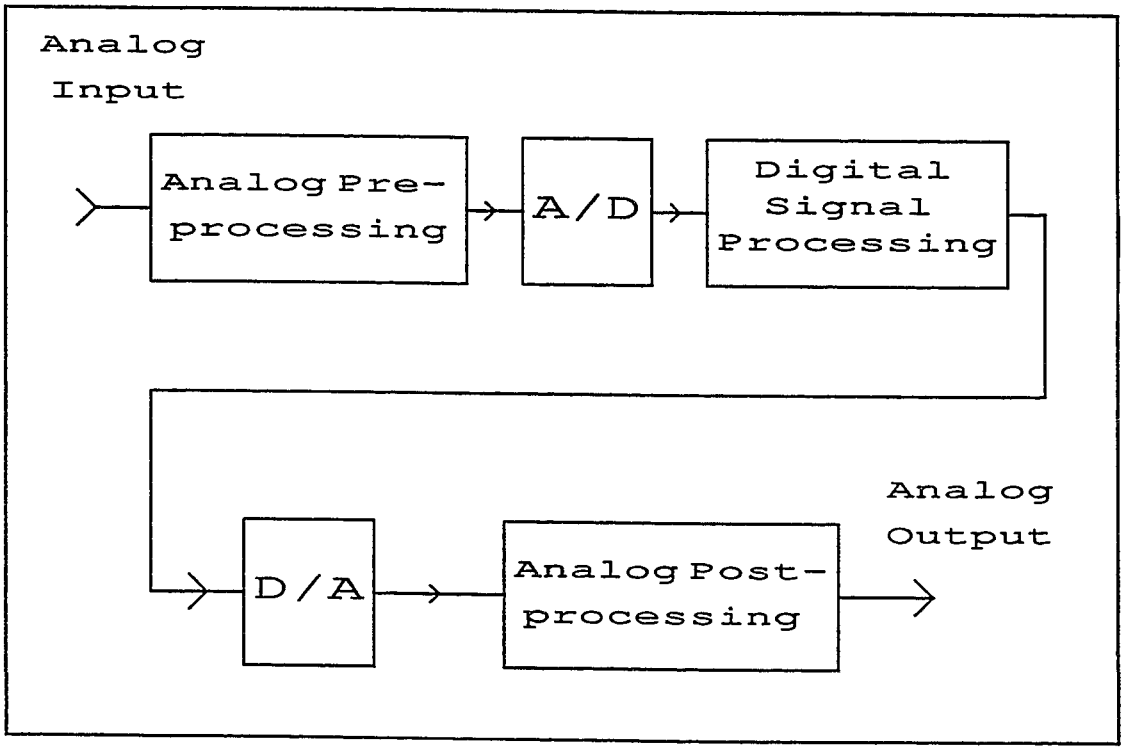

Fig. 1. Signal Processing System

To improve performance a track and hold (T/H) circuit can be added before the quantizer. Its function is to follow the input signal during the tracking time and to hold a fixed level at the quantizer's input while the

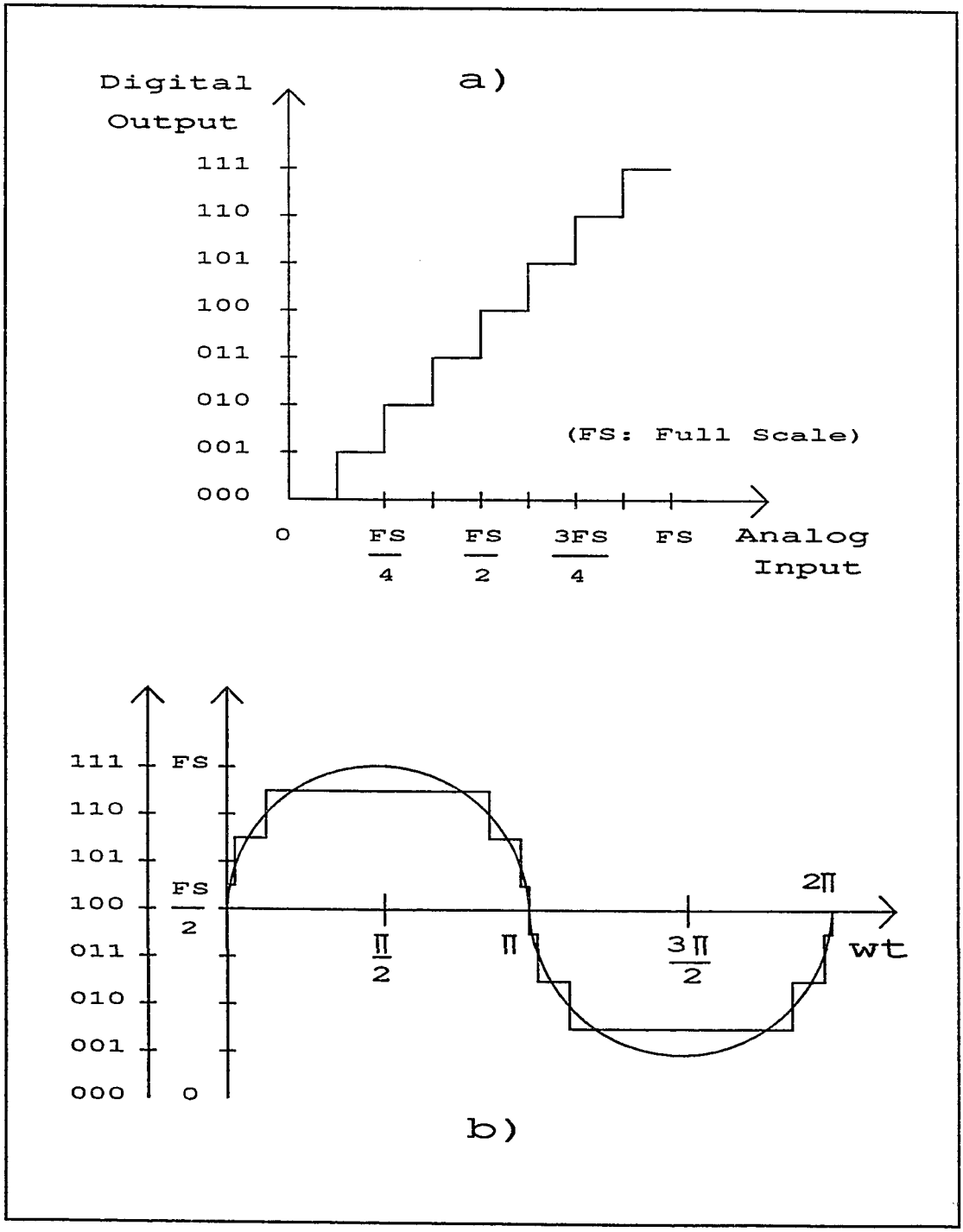

Fig. 2. Quantization. a) 3 bits quantizer transfer function; b) Quantization example

quantization process takes place. Another important function is to prevent loading of the signal source by the A/D interface. Fig. 3 shows an example of a T/H input and output.

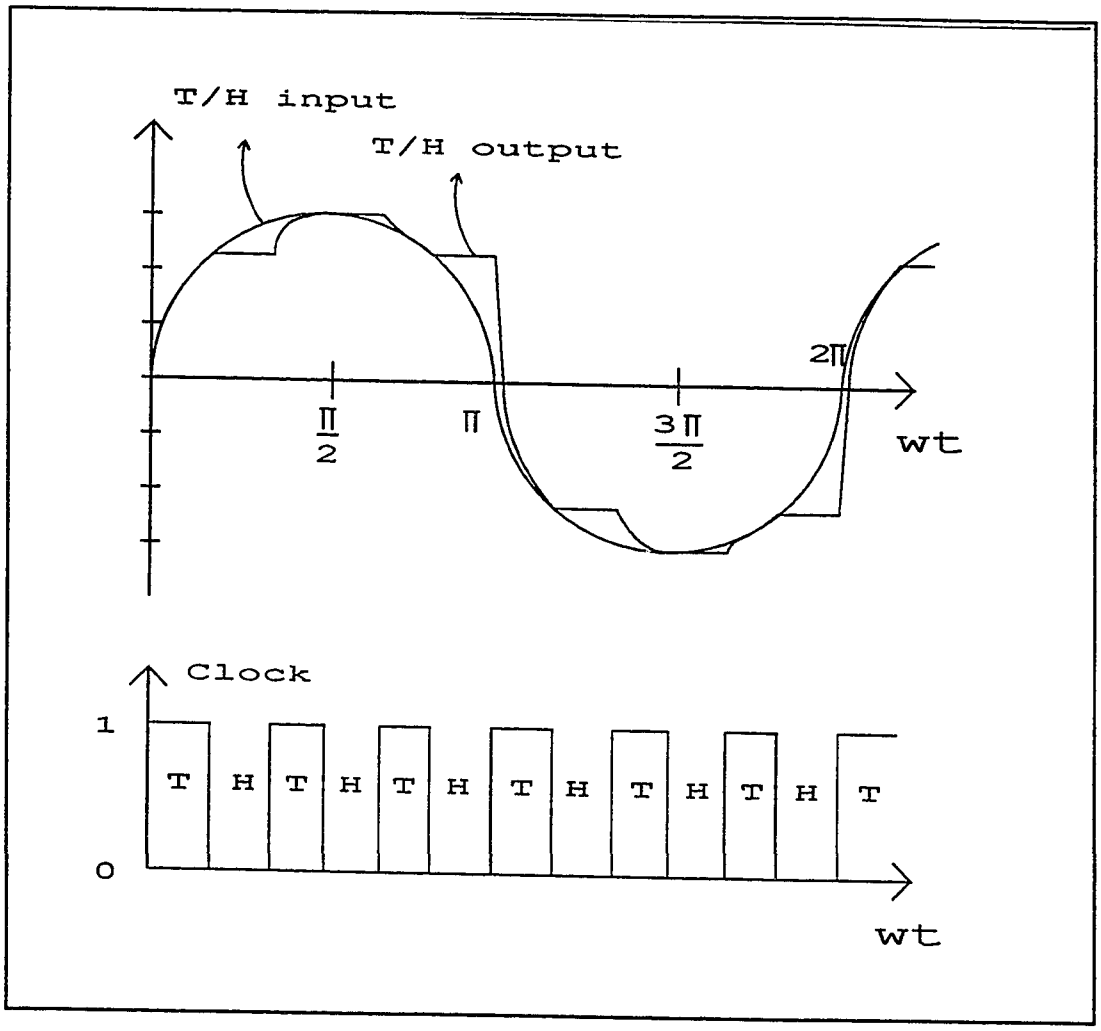

Fig. 3. Track and Hold Input and Output

In the following sections, some A/D converter architectures are described.

1.1 *Integrating A/D Converters*

The idea of this kind of converters is to use the input signal to charge a capacitor for a known interval T, so that the amount of stored charge is proportional to the average of the input signal during that interval. Then the capacitor is discharged using a reference current. The zero crossing time is proportional to the previously stored charge and consequently to the input signal. The digital output is obtained by controlling a digital counter with the discharging ramp [1]. An example is shown in fig. 4.

The accuracy of the conversion depends on matching between components and time intervals. It is independent of their actual values because they appear in both, charging and discharging ramps, and cancel out when calculating a relative interval. Integrating A/D converters are highly linear and simple, which make them a very inexpensive option.

For the maximum input values, 2^{n+1} periods of the counter are needed for one conversion (n being the number of bits). Hence, this converters are only suited for slow conversion rates, no more than hundreds of Hz.

1.2 *Counter-Comparator A/D Converters*

In these converters the input signal is compared with a stairs-like signal generated by a D/A converter that is

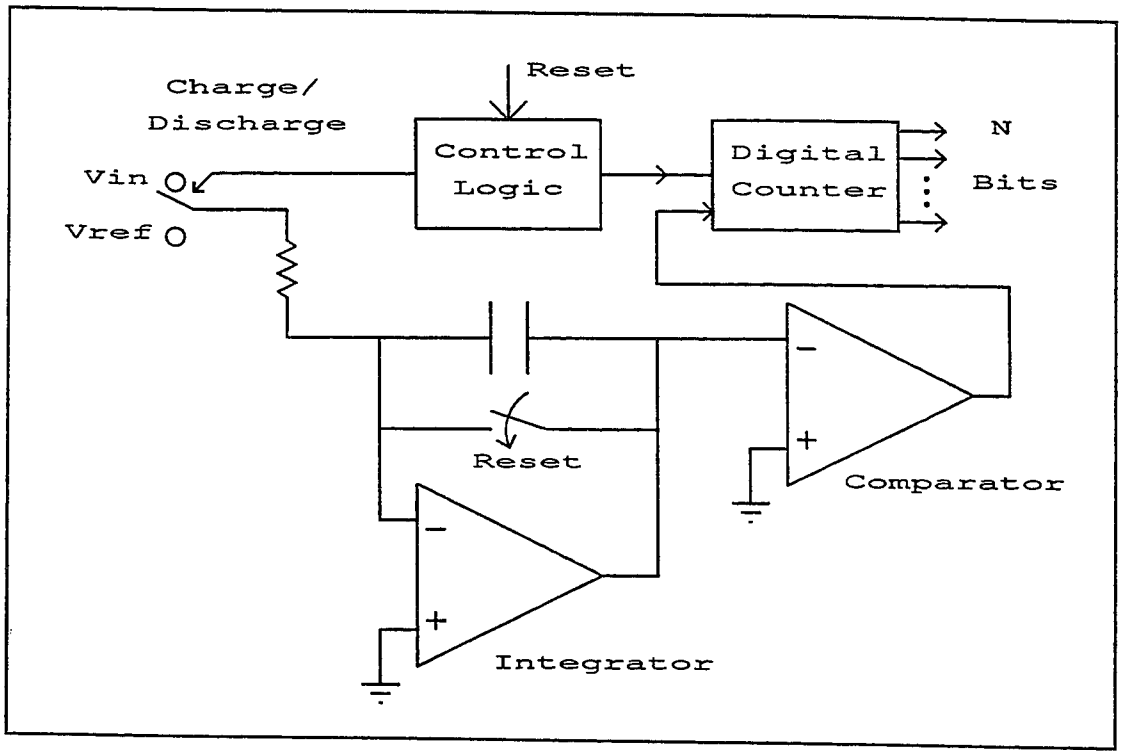

Fig. 4. Integrating A/D Converter

controlled by a digital counter. The output is given by the counter at the time that the stairs cross the input. Then, the counter is reset and a new conversion begins (fig. 5) [1].

The system is also slow for the same reason as integrating converters.

1.3 *Successive Approximations A/D Converters*

The name of these converters is very descriptive, since the digital equivalent of the incoming analog input is obtained successively, one bit at a time, beginning with the

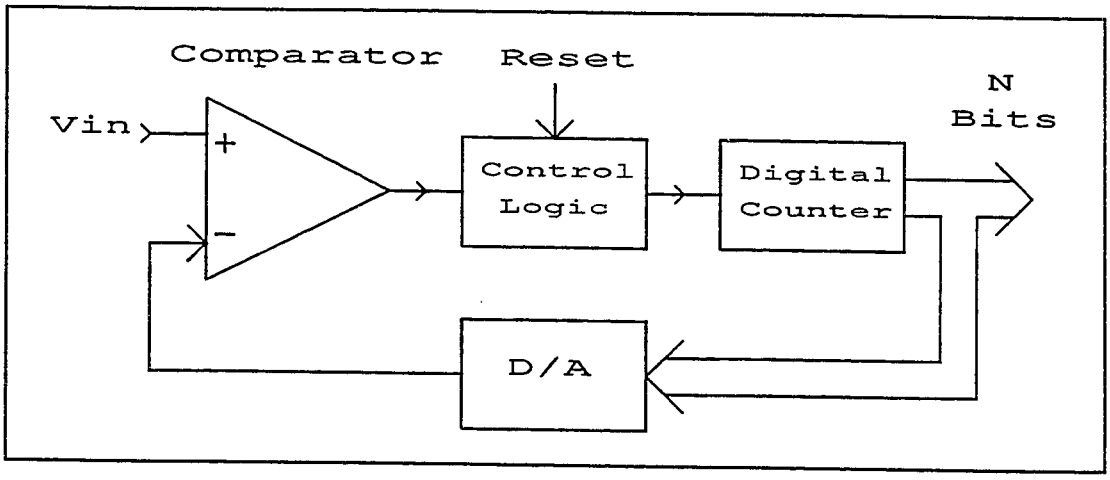

Fig. 5. Counter-Comparator A/D Converter

most significant bit (MSB), and ending with the least significant bit (LSB).

The process involves dividing the analog input range in two sectors, and deciding whether the input is in the upper or lower sector (MSB equal 1 or 0 respectively). The corresponding sector is kept, and divided again to make the decision about the second bit. The conversion ends after n iterations (n being the number of bits). In practice, the value of the reference voltage at the input of the comparator starts at one-half of the full scale and is then changed according to the result of the previous comparison [2,3,4].

The conversion always takes n clock periods, and it can provide a speed of a few MSamples/s and with high resolution (fig. 6).

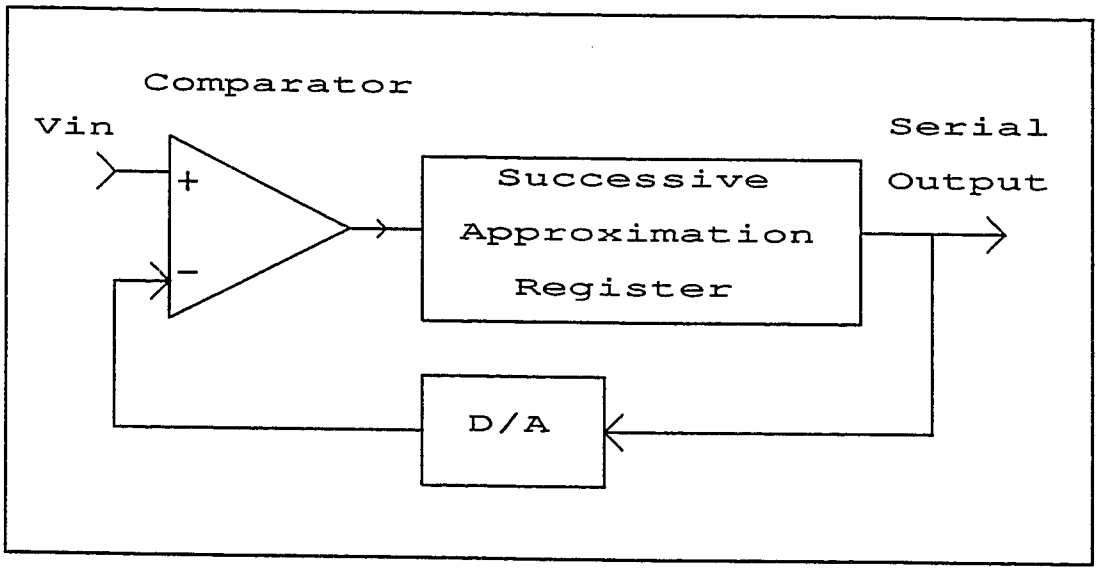

Fig. 6. Successive Approximations A/D Converter

A sample or a track-and-hold circuit is of primary importance for all but the lowest frequencies, to keep the input stable while the conversion is taking place, thus preserving the accuracy of the converter.

Resolution and accuracy are limited by the matching of the passive components and the accuracy of the D/A converter. Also, the characteristics of the comparator, such as offset and noise, affect the accuracy of the conversion.

1.4 *"Flash" A/D Converters*

Flash converters are one step fully parallel converters [5,6,7,8]. They consist of 2^n-1 comparators configured in parallel. The incoming signal is compared with the same

amount of reference levels. All comparators with references less than the incoming signal output a high level, and the others output a low level. These thermometer code is then translated to an n-bit binary code (fig. 7).

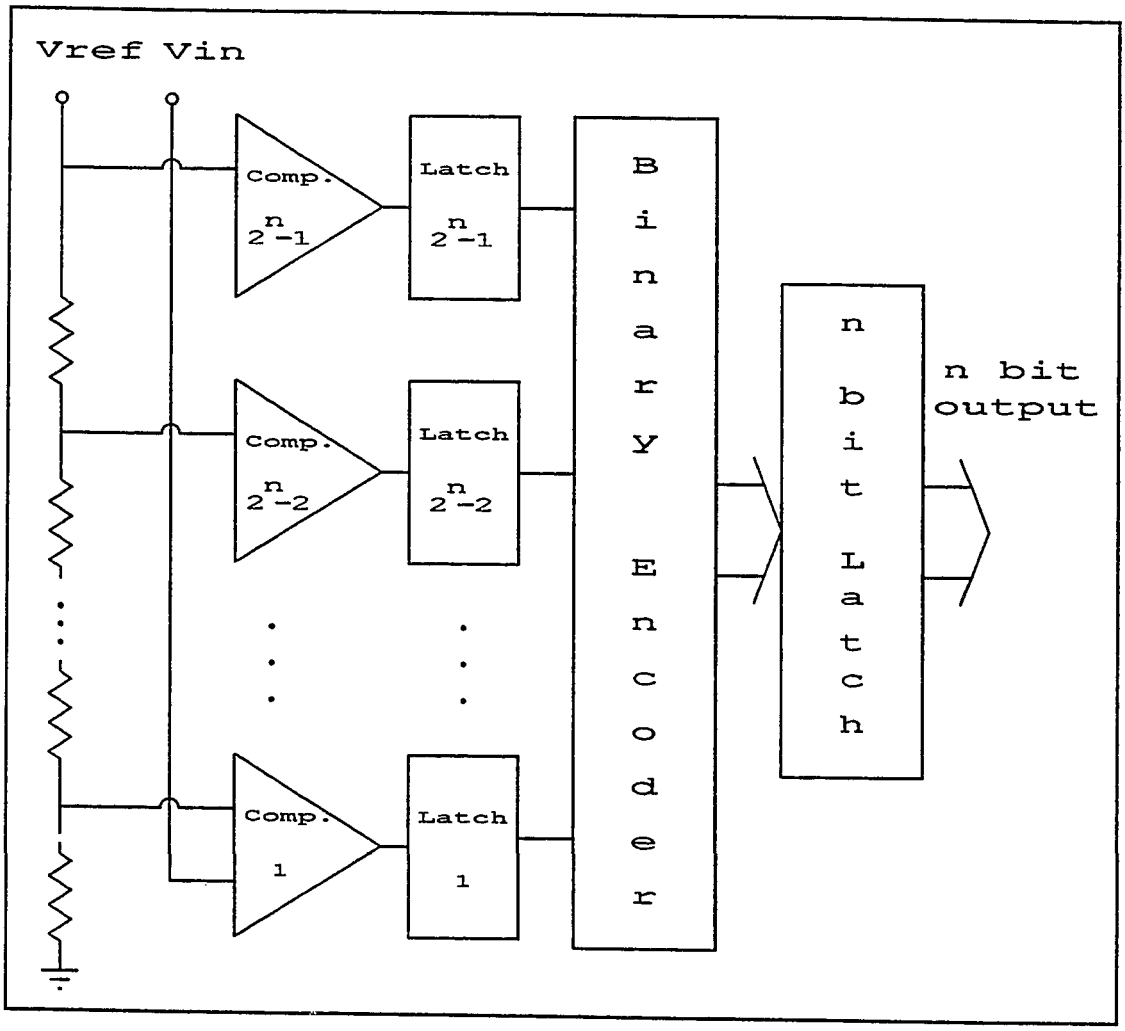

Fig. 7. Flash A/D Converter

The one step characteristic make them the fastest known architecture, with the limiting factor being the comparator speed. The fact that the number of comparators, and

consequently the die area and power dissipation increases exponentially with the number of bits, limit their practical use to no more than 8-bit converters.

Track-and-hold circuits are employed to increase resolution and to deal with the high input capacitance created by the large amount of comparators [1].

Individual references are generated by dividing a master reference with a resistor string or a capacitor array; so, the linearity is dependent on the matching between taps or the ratioed capacitors [9,10].

1.5 *Subranging A/D Converters*

Subranging A/D Converters combine flash and successive approximations architectures by dividing an n-bit conversion in m steps. Each step gives n/m bits of the total n (fig. 8).

They trade die area for speed, since the conversion takes m cycles while the amount of comparators is reduced to $2^{n/m}-1$. The comparator array and the resistor string can be shared by the successive steps. Practical converters are designed up to 12 to 14 bits in two steps [11,12,13].

1.6 *Pipelined A/D Converters*

Pipelined are an improved version of the subranging A/D converters. A sample-and-hold and gain circuit is added

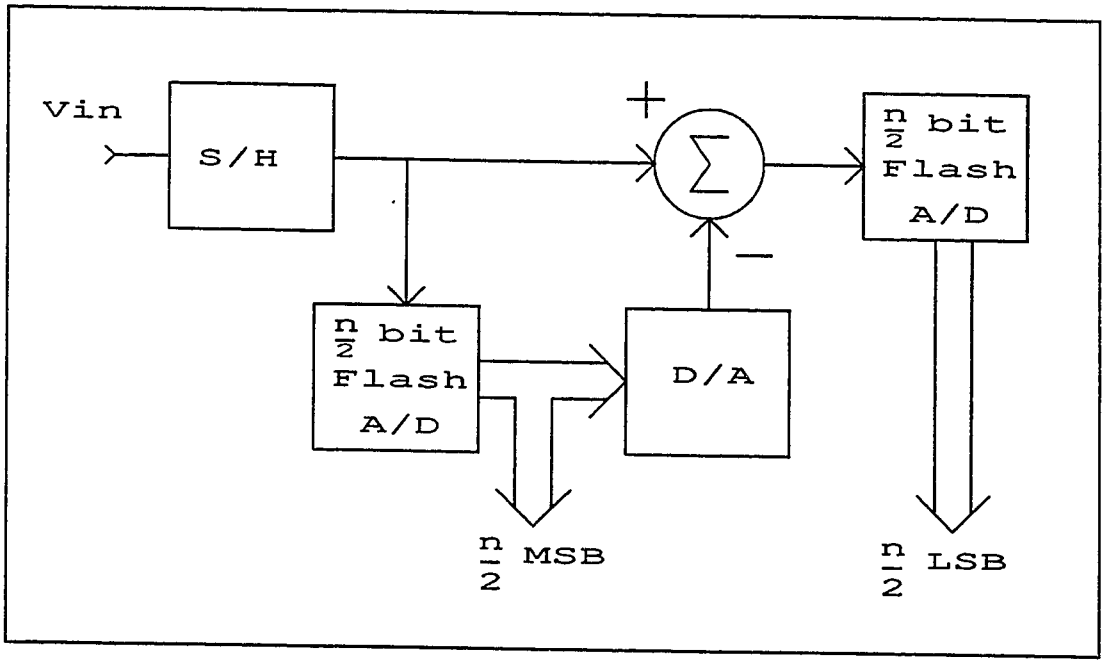

Fig. 8. Two Step Subranging A/D Converter

between stages. In this way, at a particular clock cycle, each stage is working on a different sample, and each flash subconverter receives a full range input signal (fig. 9).

The high throughput rate of pipelined converters is independent of the number of stages, but more time is necessary to transfer the residues from one stage to the following with enough accuracy. The area increases linearly with the number of stages rather than exponentially.

The interstage gain attenuates the nonlinearity effects of the stages following the first one. Also, digital correction is used to compensate for nonlinearities and offset of those stages [14]. In this way, the precision of the first D/A converter and the first interstage gain

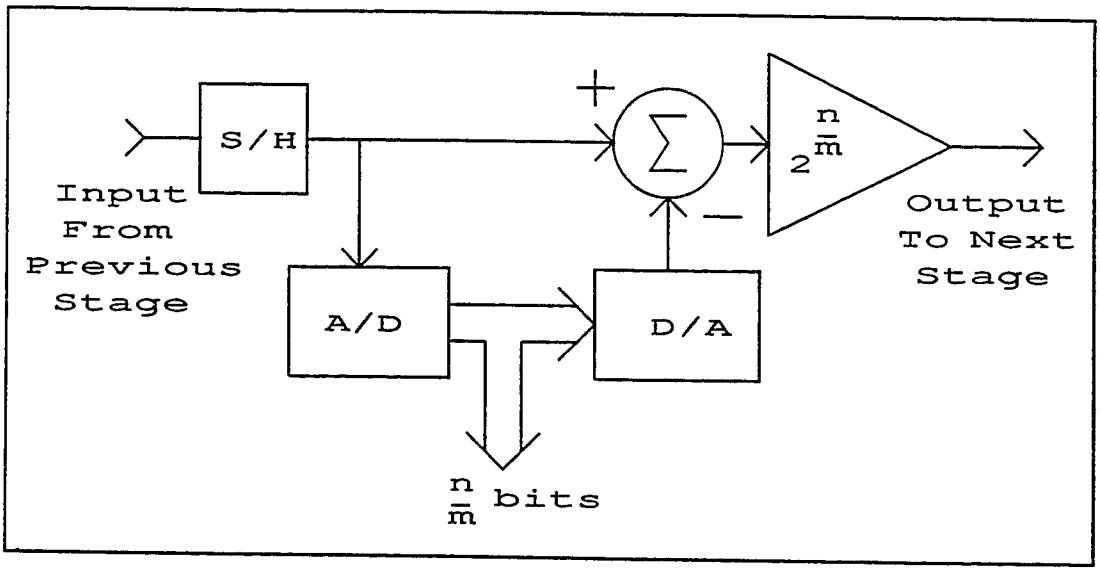

Fig. 9. One Stage of a Pipelined A/D Converter

determine the linearity of the whole converter [15,16,17,18].

1.7 *Oversampled A/D Converters*

Oversampled A/D converters exchange resolution in time for resolution in amplitude. A first or second order Sigma-Delta modulator containing one or two analog integrators, a two level quantizer, and a D/A converter in a feedback loop, samples the analog input at several times the Nyquist frequency. As the sampling frequency increases, the total quantization error stays the same, whereas its density decreases by spreading it over a higher frequency range. The modulator is followed by a digital low-pass filter that

eliminates the out-of-band noise and quantization error, and outputs a Nyquist rate bit stream (fig. 10).

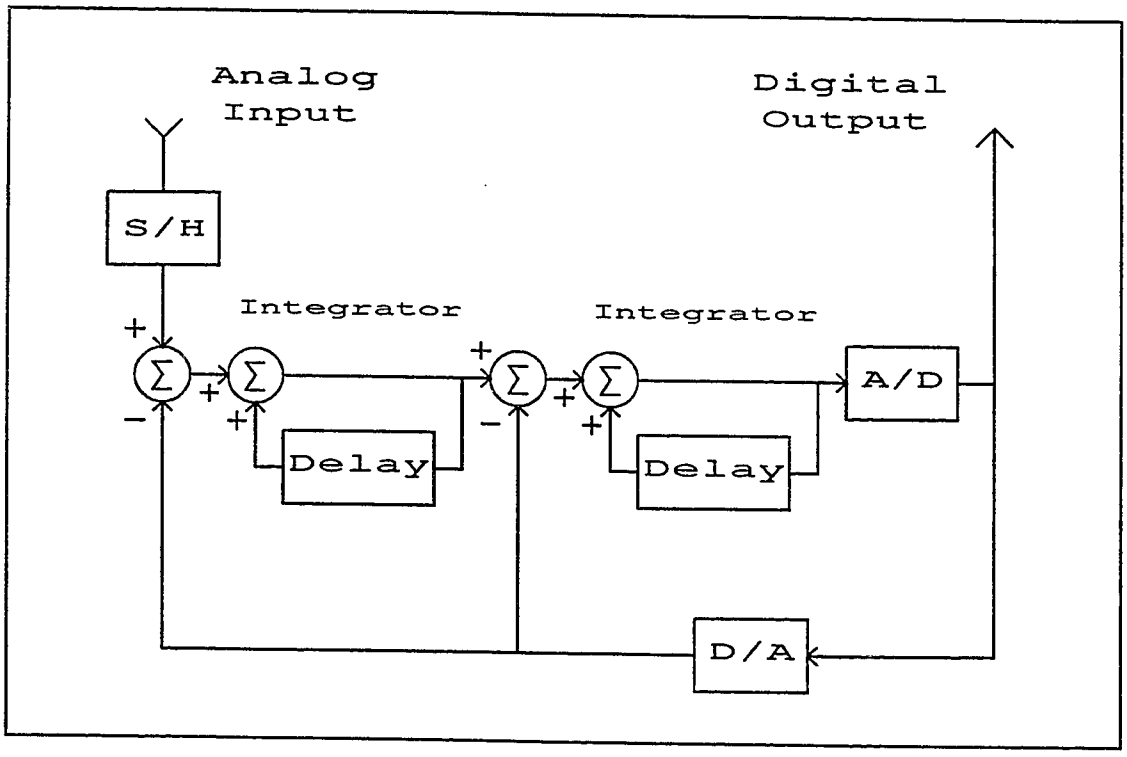

Fig. 10. Second Order Oversampled A/D Converter

The main advantage of oversampled converters is that they do not need precision analog components because they use a simpler two level quantizer. Consequently, they are an excellent option to integrate in technologies optimized for high speed digital circuitry. Also, the anti-alias filter is less critical due to the high sampling rate.

The limitation comes from the fact that as video frequencies and high resolution are required, sampling rates become too high for present technologies [19,20,21,22].

CHAPTER 2

Converter Design

The goal for this circuit is to achieve video conversion rates with an accuracy of 8 bits, by utilizing a 3.3V±10% power supply, in a BiCMOS technology. The technology includes a 4GHz NPN bipolar transistor and both P and N-type MOSFETs. The minimum drawn channel length is 2μm.

In video applications, the composite signal is sampled at four times the frequency of the color subcarrier, which is 3.58MHz in NTSC systems, or 4.43MHz in PAL systems. Therefore the sampling rates are 14.32 or 17.72MSamples/s respectively. This converter is designed to be used with either video standard.

Previous works [18,23,24,25,26,27,28,29,30], have shown that the above mentioned objectives are feasible. The difficulty from operating with only a 3V power supply is dealt with by circuit techniques, and the availability of a BiCMOS technology.

The input capacitance of a flash ADC is the sum of the contribution from all those of the 2^n-1 comparators; with n being the number of bits the converter resolves. To deal with this large capacitance, a track-and-hold circuit (T/H)

is used. A T/H amplifier also enhances a flash ADC performance by presenting a set of successive dc voltages to the comparators, instead of the high slew-rate input signal [31].

Fig. 11 shows a conceptual block diagram of the whole system. It is designed to work with a single clock. All the required clock phases are generated internally as explained in chapter 5. During the first half of the clock period switches Sa and Sb are connected to the output of the T/H amplifier, while Sc, Sd, Se, and Sf are closed. The incoming analog signal is sampled on the sampling capacitors, and at the same time the comparator amplifiers' offset is sampled on the offset cancellation capacitors. In the next half clock period, Sa and Sb are connected to the corresponding taps on a reference resistor string, while Sc, Sd, Se, and Sf are opened. The voltage previously sampled on the sampling capacitors is subtracted from the references and the result is applied to the inputs of the comparator amplifiers. After a significantly large differential signal is developed at the input of the comparator latches, these circuits become active and the result of each comparison is stored. The result will be in thermometer coding, with digital ones for all the comparisons whose references are less than the sampled analog signal, and digital zeros for the others, totaling 2^n-1 binary digits. At the following

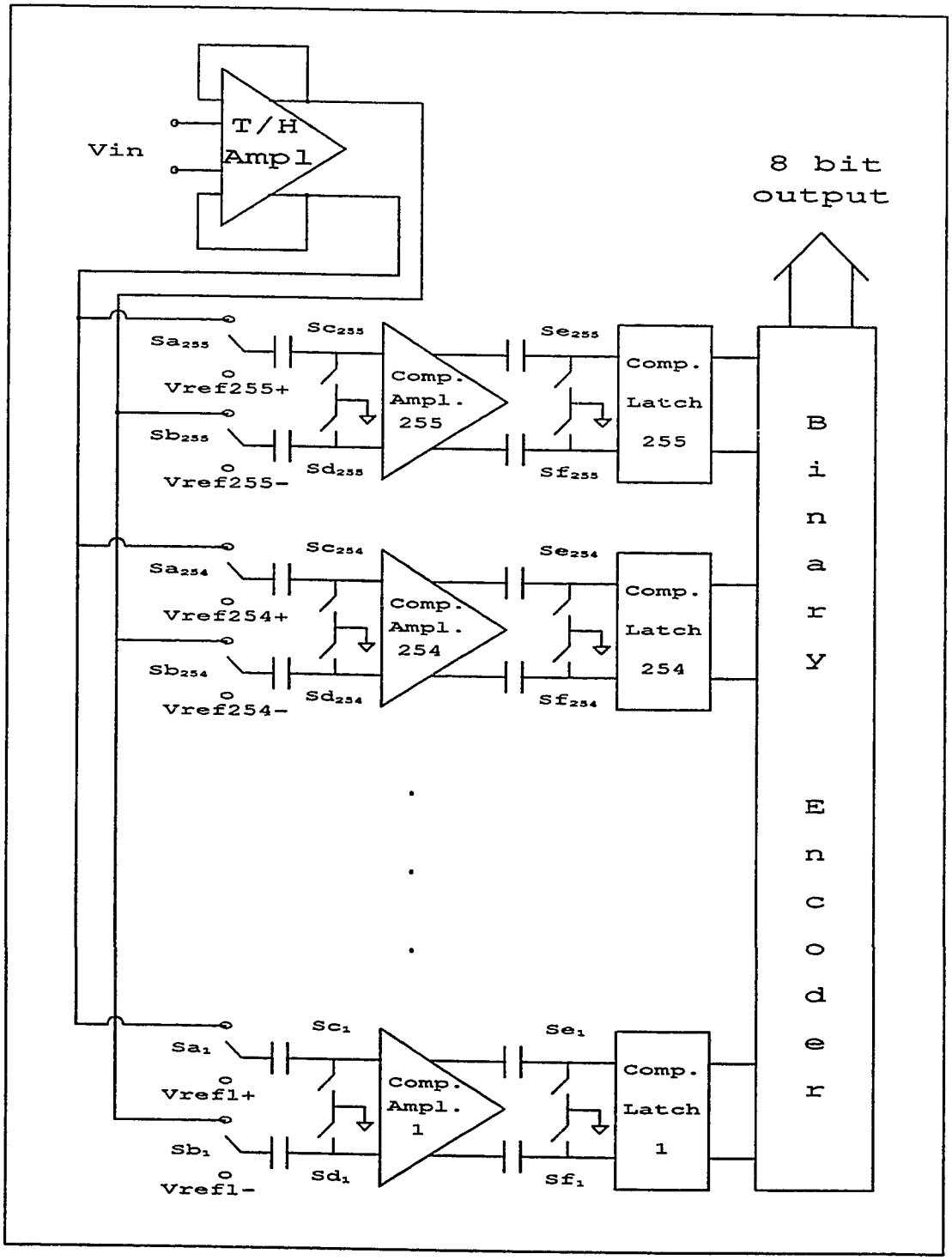

Fig. 11. Conceptual Fully Differential Flash ADC with T/H

clock period, error correction and code conversion takes place, and finally, an 8-bit word is ready for further digital processing.

For the fastest sampling rate of 17.72MHz the period is T_s=56.43nsec. Substracting the switching transient times between modes of operation, there are 24ns for the T/H amplifier to settle and for the comparator to reset, 12ns for the comparator's amplifier to settle, and 12ns for the regenerative latch to settle.

The following sections analyze some of the characteristics that contribute to the uniqueness of this circuit design. Finally, some SPICE parameters are given along with the models that are used for hand calculations.

2.1 *Fully Differential Configuration*

Both the T/H operational amplifier and the comparators are fully differential. The main advantages of using fully differential configurations rather than single ended are better power supply rejection (PSRR), common mode rejection (CMRR), and dynamic range. On the other hand, single ended configurations are simpler, do not need common mode feedback circuits but they need differential to single ended converters.

For a fully differential circuit, a common mode signal, i.e., applied simultaneously to both signal paths, does not

produce any output, and any noise that is symmetrically coupled is rejected as well. The previous statements are true provided that the circuit and layout are symmetric, and that there is no component mismatch. But even with some mismatch the improvement is very significant. This characteristic of rejecting noise is certainly important when talking about mixed signal circuits, i.e., analog and digital, where the clock feedthrough, caused by fast switching, can greatly disturb the analog sections. In addition, the dynamic range at differential processes is doubled, since the input referred noise is essentially the same, while the maximum amplitude of the effective signal, given by the difference of two equal amplitude but opposite phase components, is doubled.

2.2 *BiCMOS Technology*

The trend to achieve larger integration has reached a point where analog and digital functions are brought together as mixed signal systems on a chip. Considering this fundamental category of applications, technologies cannot anymore be chosen either for building digital or for building analog circuitry. Digital designs required scaled MOSFETs to achieve high packaging densities, while high speed analog functions favor the use of bipolar transistors. Nevertheless, both kinds of applications benefit with the

availability of MOSFETs and BJTs in the same process. In addition,some BiCMOS technologies provide dual-polysilicon capacitors and thin-film resistors which are high-quality passive components.

Bipolar transistors have the following relative advantages: Excellent matching properties between adjacent devices, low noise, low offset, wide bandwidth, high and predictable transconductance, they are very stable with small dependence on surface-related effects, and are suitable for translinear circuit techniques.

On the other hand, MOS transistors have the following properties: Zero DC current, good n and p-type complementary devices, zero offset switches, and extremelly high input resistance which makes the gate an excellent charge storage node [32,33,34,35,36].

2.3 *Low Voltage Power Supply*

During the last six years, many areas of the integrated circuit industry have been moving from the 5V power supply standard toward a 3.3V standard, and some are already moving to lower voltages. The leading sectors in this trend are those involved in memory circuit design, but companion digital and analog circuits are finally also in the market [37,38,39,40].

The main reasons for the supply voltage shift are to allow for more and more transistor density maintaining a reasonable power dissipation, and to increase portable device size, weight, and autonomy. At the same time, reducing heat generation translates in less packaging and cooling cost, and components reliability is enhanced. Also, as transistor dimensions are scaled down, hot-carrier effects become critical and reducing the supply voltage is ultimately necessary.

However, those advantages bring, simultaneously, many other circuit design challenges to overcome. The available overdrive voltage (Vgs-Vt) for a MOSFET is reduced, decreasing the transistor current and therefore the speed. Threshold voltage variations are more significant and noise margins are smaller. For BiCMOS inverters the situation is worse, since traditional configurations are not full swing designs. Therefore new logic gates have to be developed [41]. For analog circuits swing and resolution are smaller. Also bandwidth and switch on-conductance, which are proportional to the overdrive, are significantly reduced.

2.4 *Transistor models*

This section shows some SPICE transistor parameters along with the models that are used in hand calculations.

The corresponding equivalent circuits are shown in fig. 12 [36,42,43].

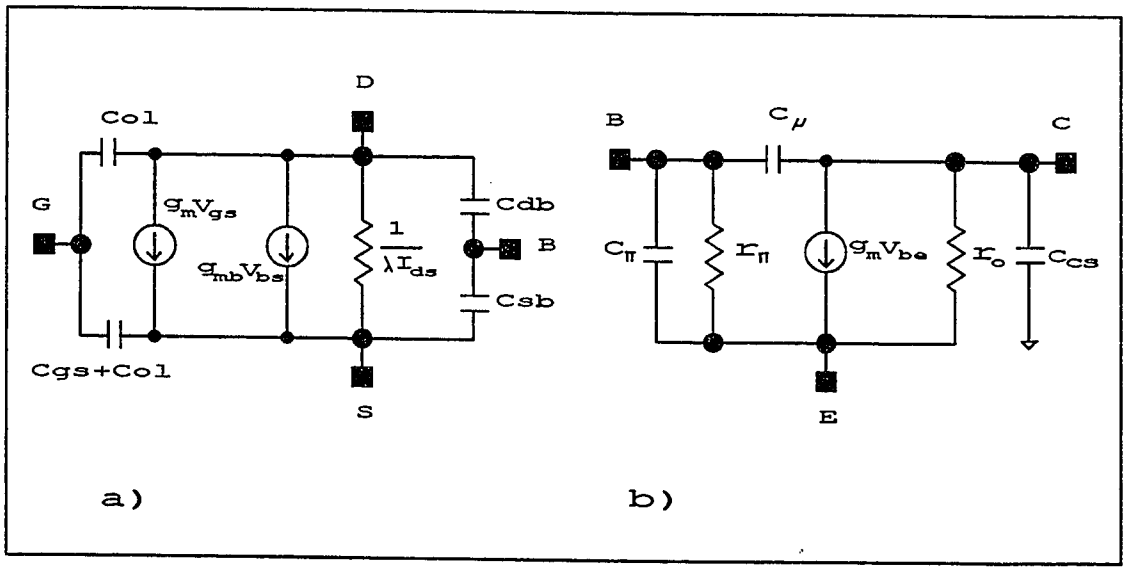

Fig. 12. Simplified Transistor Equivalent Circuits in Forward Bias Operation Region. a) MOSFET; b) BJT

2.4.1 *MOS Transistors*

Param.	NMOS	PMOS	Param.	NMOS	PMOS
VTO	0.3V	-0.3V	CGSO	0.3fF/μm	0.3fF/μm
KP	61μA/V^2	23μA/V^2	CGDO	0.3fF/μm	0.3fF/μm
GAMMA	0.2V$^{1/2}$	0.6V$^{1/2}$	CGBO	0.38fF/μm	0.37fF/μm
LD	0.25μm	0.25μm	CJ	0.09fF/μm^2	0.3fF/μm^2
TOX	418Å	418Å	MJ	0.78	0.56
CJSW	0.55fF/μm	0.3fF/μm	PB	0.8V	0.8V
MJSW	0.28	0.24			
LAMBDA	0.018V^{-1}*1.5μm/Leff (NMOS)				
LAMBDA	0.05V^{-1}*1.5μm/Leff (PMOS)				

$$Cox = \frac{\epsilon OX}{TOX} = 0.83 fF/\mu m^2$$

$$COX = W\,(L - 2\,LD)\,Cox$$

$$Col = CGSO = CGDO = 0.3 fF/\mu m$$

$$COL = W\,Col$$

$$CBS = CJ \frac{AS}{\left(1 - \frac{Vbs}{PB}\right)^{MJ}} + CJSW \frac{PS}{\left(1 - \frac{Vbs}{PB}\right)^{MJSW}}$$

$$CBD = CJ \frac{AD}{\left(1 - \frac{Vbd}{PB}\right)^{MJ}} + CJSW \frac{PD}{\left(1 - \frac{Vbd}{PB}\right)^{MJSW}}$$

2.4.2 *Bipolar Transistor*

Param.	Value	Param.	Value	Param.	Value
IS	0.08fA	BF	80	VAF	70V
IKF	10mA	RB	1200Ω	RBM	13Ω
IRB	30μA	RC	750Ω	RE	17Ω
CJE	100fF	MJE	0.5	VJE	0.85V
TF	40ps	CJC	100fF	MJC	0.5
VJC	0.8V	CJS	180fF	MJS	0.2
VJS	0.7V				

$$r_\pi = \frac{\beta}{gm} = \frac{2.6V}{Ic}$$

$$r_o = \frac{VA}{Ic} = \frac{70V}{Ic}$$

$$C_\pi = 2\,Cje + \tau_F gm = 200fF + 1.54ns/V\,Ic$$

$$C_\mu = \frac{CJC}{\left(1 - \frac{Vbc}{VJC}\right)^{MJC}} = \frac{100fF}{\left(1 - \frac{Vbc}{0.8V}\right)^{0.5}}$$

$$Ccs = \frac{CJS}{\left(1-\frac{Vsc}{VJS}\right)^{MJS}} = \frac{180fF}{\left(1-\frac{Vsc}{0.7V}\right)^{0.2}}$$

CHAPTER 3

Comparator Design

The comparator consist of three stages: a sampling switch capacitors input section, a preamplifier, and a latch. This chapter focuses on the design of each of the above stages.

The function of a comparator is to decide if a given voltage is larger or smaller than a reference voltage. The minimum differential voltage that it can resolve directly affects the accuracy of the converter. This function is usually realized by linear preamplification followed by regenerative amplification. The purpose of the first one is to overcome any static and dynamic offset at the input of the regenerative latch. The dc offset of the amplifier is cancelled out in this design by storing it at the interstage capacitors during the calibration time.

3.1 *Comparator's Input Section*

The comparator's input section is shown in fig. 13. During the first phase of the clock ϕ_1, the sampling capacitors are connected between the outputs of the T/H amplifier and the common mode reference voltage BIAS7. The voltage across these capacitors tracks the analog input.

When $\overline{\phi_1}$ goes high, transistors MI1 and MI2 are turned off, and since the charge at the amplifier's input node is

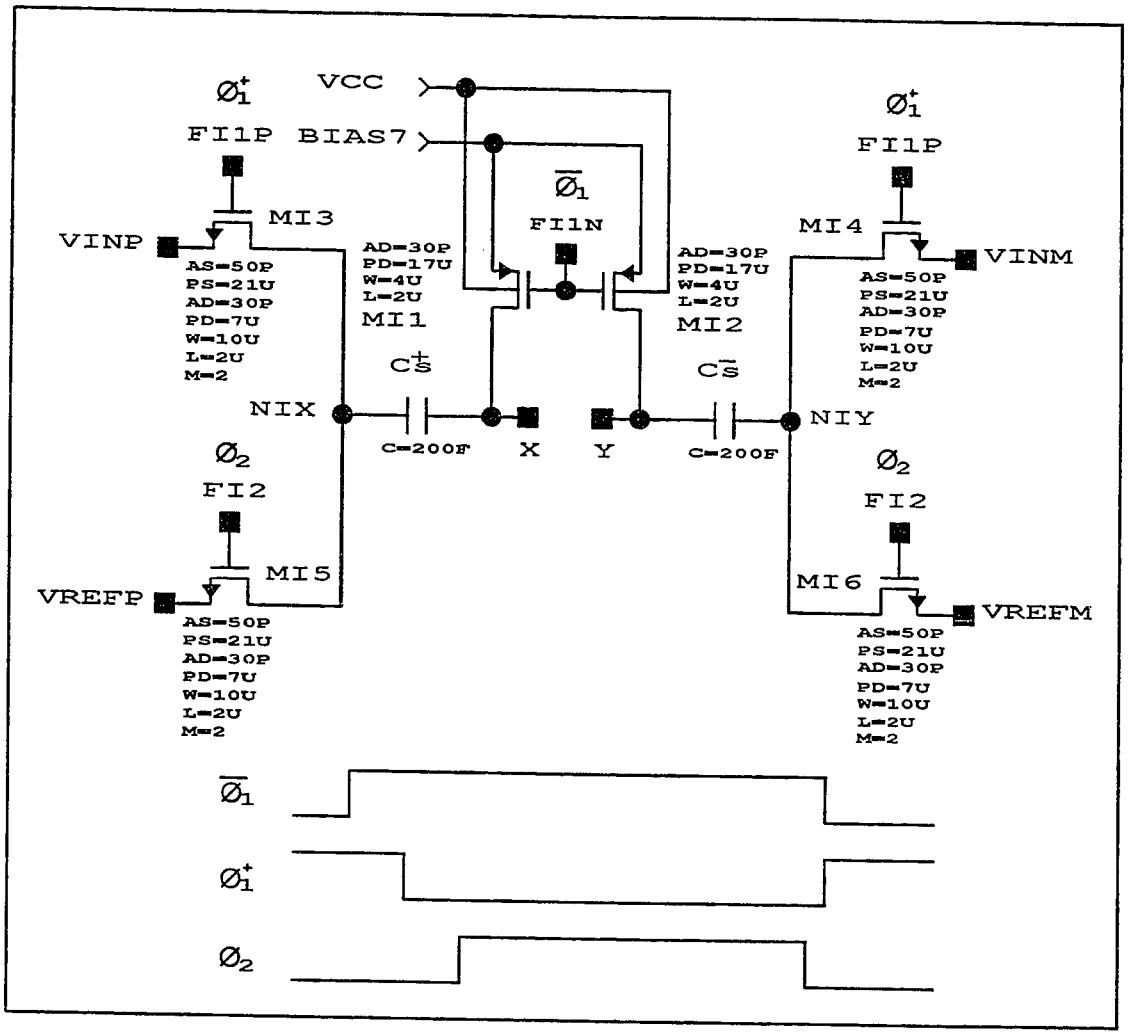

Fig. 13. Comparator's Input Section

conserved, the voltage across the capacitors remains constant. The net effect is the sampling of the analog input on C_s^+ and C_s^-. Then, ϕ_1^+ goes low disconnecting the other plates of the capacitors from the input, and finally,

ϕ_2 goes high to connect them to the corresponding

reference voltage. At this point a substraction takes place, and the difference between the reference voltage and the applied input signal is amplified by the comparator's amplifier stage [44,45,46].

$$V_{id} = V_x - V_y$$

$$V_{id} = (V_{ref}^{+} - V_{in}^{+}) - (V_{ref}^{-} - V_{in}^{-})$$

$$V_{id} = \Delta V_{ref} - \Delta V_{in}$$

If the clock sequence were altered, turning on MI5 and MI6 before turning off MI1 and MI2, the voltage across the sampling capacitors would no longer be a sample of the analog input. Or if ϕ_1^{+} were still high when ϕ_2 goes low, a current path would be formed between the reference resistor string and the T/H amplifier's output disturbing the system and increasing the settling time.

The voltage Vid is not completely applied to the input of the comparator's amplifier. It is partially attenuated by the voltage divider between C_s, and the input capacitance of the amplifier plus the parasitic capacitances at nodes X or Y. C_s has to be big enough so that the effective V_{id} is not attenuated in excess. For this design C_s^{+} and C_s^{-} are 150fF and the attenuation is about 20%.

Charge injection from MI1 and MI2 is mainly a common mode component and generates only a negligible differential component. The differential charge injection is due to mismatches between transistors MI1 and MI2, and also to differences in the impedance seen from their terminals. In this design the magnitude of the differential charge injection is sufficiently small so as not to cause any nonlinearity as converter offset, but it is a significant concern in higher resolution converters [47,48].

The voltage feedthrough is also mainly a common mode component, and as charge injection, it does not affect the signal. Nevertheless, it can cause big transients that can turn off the amplifier's input transistors, slowing the process, and can also turn on the parasitic diodes between the drain and substrate of MI1 and MI2. To deal with this problem C_s may be increased, or the common mode reference may be adjusted to leave enough headroom for the expected transients.

The references for the 255 comparators are generated with a resistor string of 127 taps. In order to illustrate the way it is implemented, fig. 14 shows an example for a 3 bit system which require $2^{3-1}=4$ taps. If the input swing is ±1V, the references are ±0.75V, ±0.5V, ±0.25V, and 0V.

When ϕ_2 goes high, the references are connected to the sampling capacitors, and a disturbance is created on the

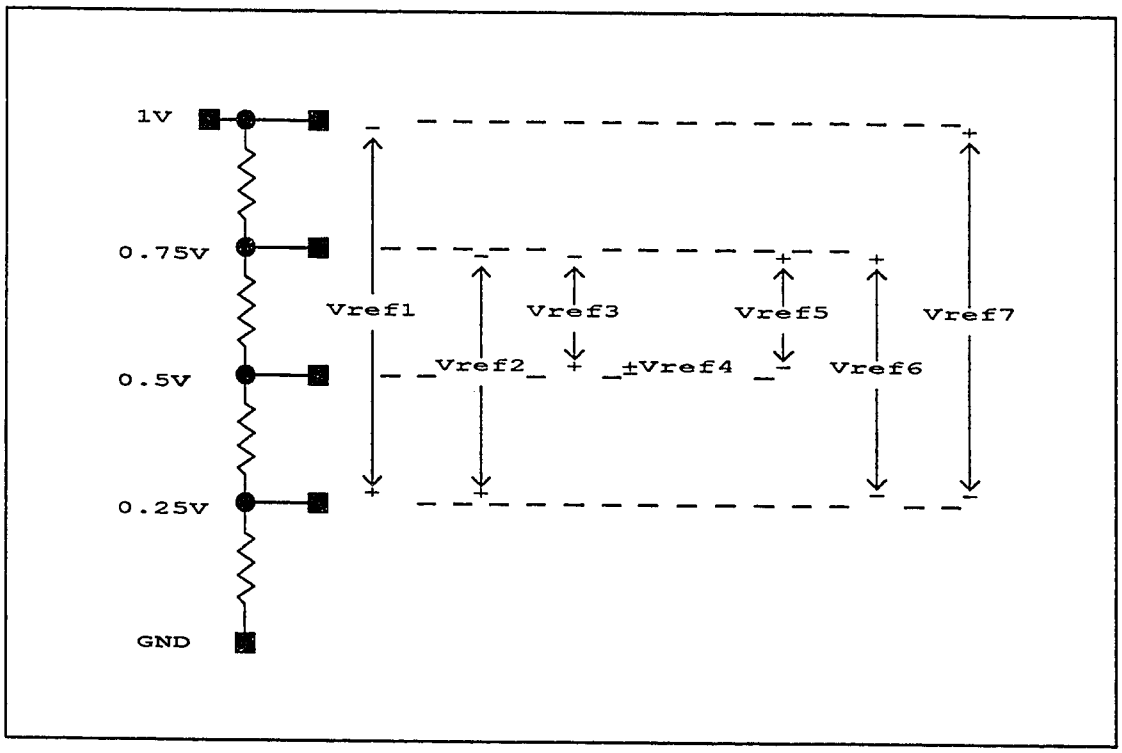

Fig. 14. Comparator's References Generation: 3 bit Example

tap's voltages. The settling time depends on the resistance and on the capacitance seen by the string. The equivalent circuit is an RC ladder network, with a capacitance connected from each tap to ground. Each capacitance is the series combination of C_s, with the input capacitance of the amplifier plus the parasitic capacitances at nodes X or Y, or about 15fF.

The allotted time for settling to a LSB/4 is 1.5ns and, for a disturbance as high as 1V, 6.2 time constants would be needed ($n = -\ln\left(\frac{2mV}{1V}\right) \approx 6.2$).

Simulations show that the slowest settling occurs when all the capacitance is placed between two halves of the total resistance, in which case the time constant is $\frac{R}{4}\times C$. As the resistance and capacitance are divided to form an RC ladder, the settling time is rapidly reduced to less than half that value.

$$\tau \leq \frac{1}{8} R_{TOTAL} C_{TOTAL}$$

$$R_{TOTAL} \cong \frac{8\tau}{C_{TOTAL}} = \frac{8 \times 1.5ns/6.2}{255 \times 40fF} = 190\Omega$$

In this design, the external reference is 1.5V, and the required tap's voltages are from 0.5V to 1.5V, in order to have the same swing as that of the T/H amplifier and keep the comparators properly biased for all input voltages. The resistor string is formed by 128 resistors of 1Ω, that provide the references every 7.8125mV, from 0.5V to 1.5V, and a 64Ω resistor between the 0.5V tap and ground. The total is 192Ω, with a total current of 7.8mA.

The matching of the resistors affects the linearity of the converter. According to Lewis [9], an upper bound for the maximum allowable resistor mismatch, $\frac{\sigma_R}{R}$, for 2^{n-1} decision levels, and N+1 bits of linearity is:

$$\frac{\sigma_R}{R} \leq 2^{\frac{(n-1)}{2} - (N+1)}$$

For n=N=8:

$$\frac{\sigma_R}{R} \leq 2^{\frac{7}{2}-9} = 2.2\%$$

3.2 *Amplifier Design*

The gain of this amplifier is determined by considering the value of the minimum input signal, and the maximum offset expected from the following stage. This design requires the circuit to distinguish a minimum input signal of LSB/4. For an input swing of ±1V and a resolution of 8 bits, that is $\frac{LSB}{4} = \frac{2V}{2^{n+2}} \cong 2mV$. Considering the presence of some residual offset, the comparators are expected to resolve an LSB/2.

This design uses a regenerative latch with bipolar inputs, which is expected to have less than 3mV of offset. On the other hand, a MOSFET based latch can have an offset of several tenth of millivolts.

In addition, there are two sources of attenuation in the signal path: One is at the output of the amplifier, due to the divider action between the offset cancellation capacitors and the capacitance of the inputs of the regenerative latch. The other attenuation comes from using an NMOS source follower, which can attenuate by as much as 20%, due to the MOSFET body effect.

To solve the trade-off of very high bandwidth, with a relatively low gain, and a small area, an emitter coupled

pair stage with resistive loads and a gain of eight is adopted. A source follower is added to the input to provide the high impedance needed to prevent the loss of charge in the sampling capacitors. This addition significantly increases the noise comparing with a purely bipolar amplifier. The comparator amplifier is shown in fig. 15.

Notice that the step response of this amplifier approaches asymptotically its final value and therefore it is preferable to have extra gain at the expense of some bandwidth to use the amplifier in the high dV_{out}/dt region .

The gain of the emitter coupled pair stage is $\frac{V_{N5-N6}}{V_{N1-N2}} = -gm_5 R_5 = -\frac{Ic}{V_T} R_5 \cong -8$, which gives a constraint on $Ic\ R_5$. The effective gain of the whole comparator's amplifier, considering 20% attenuation on M1 and M2, and $C_{of} = 3C_{11}$ is: $G \cong -0.8 \times 8 \times 0.75 = -4.8$.

It is very important to keep the gain independent of temperature and resistor value. That is because both are subject to broad variations. Notice that the gain is directly proportional to the collector current and resistor value, and inversely proportional to the absolute temperature ($V_T = kT/q$). Therefore, if the bias current is made inversely proportional to the resistance and directly proportional to the absolute temperature, then these variables are cancelled out, and the gain becomes independent of temperature and absolute resistance value,

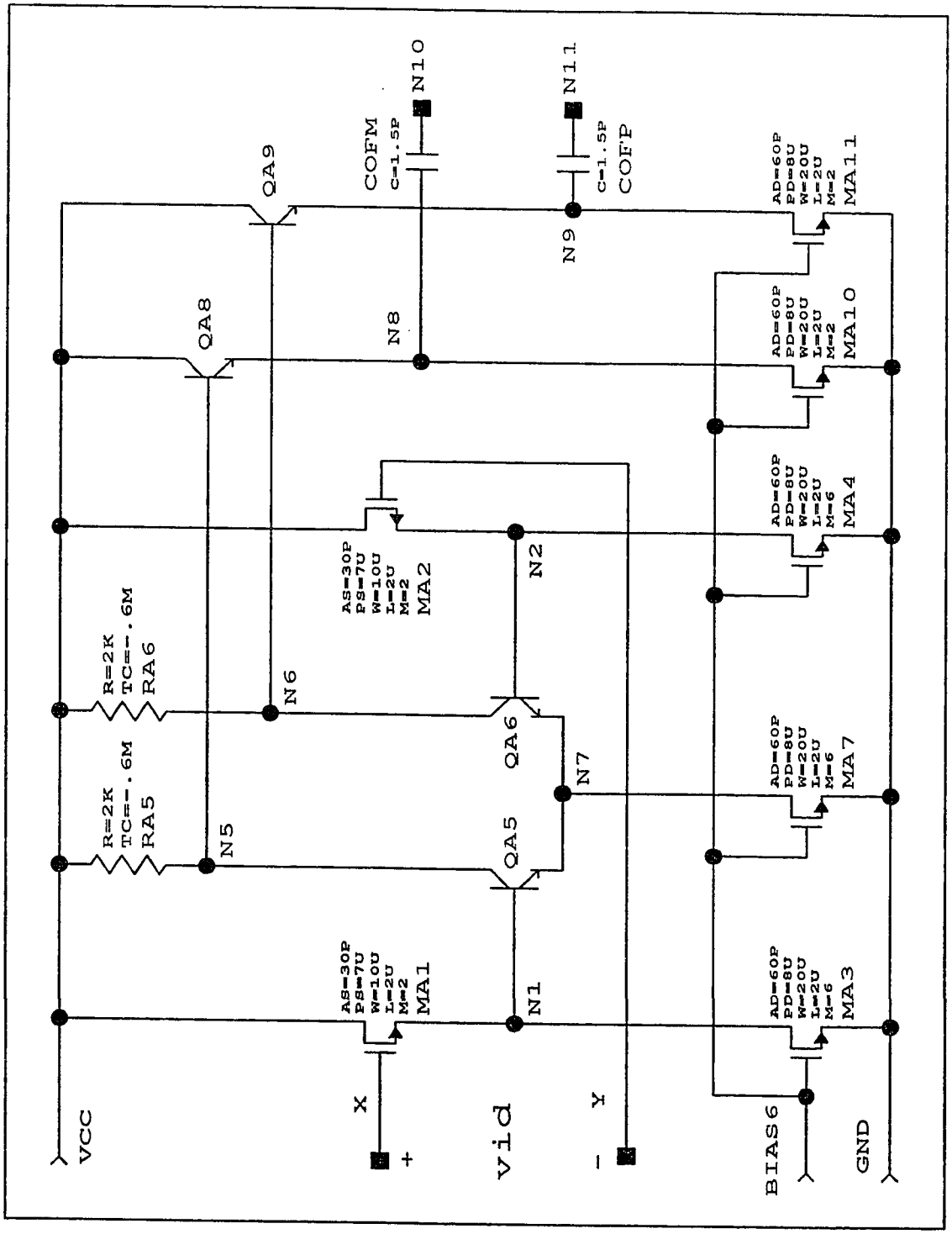

Fig. 15. Comparator's Amplifier

and only dependent on resistance matching.

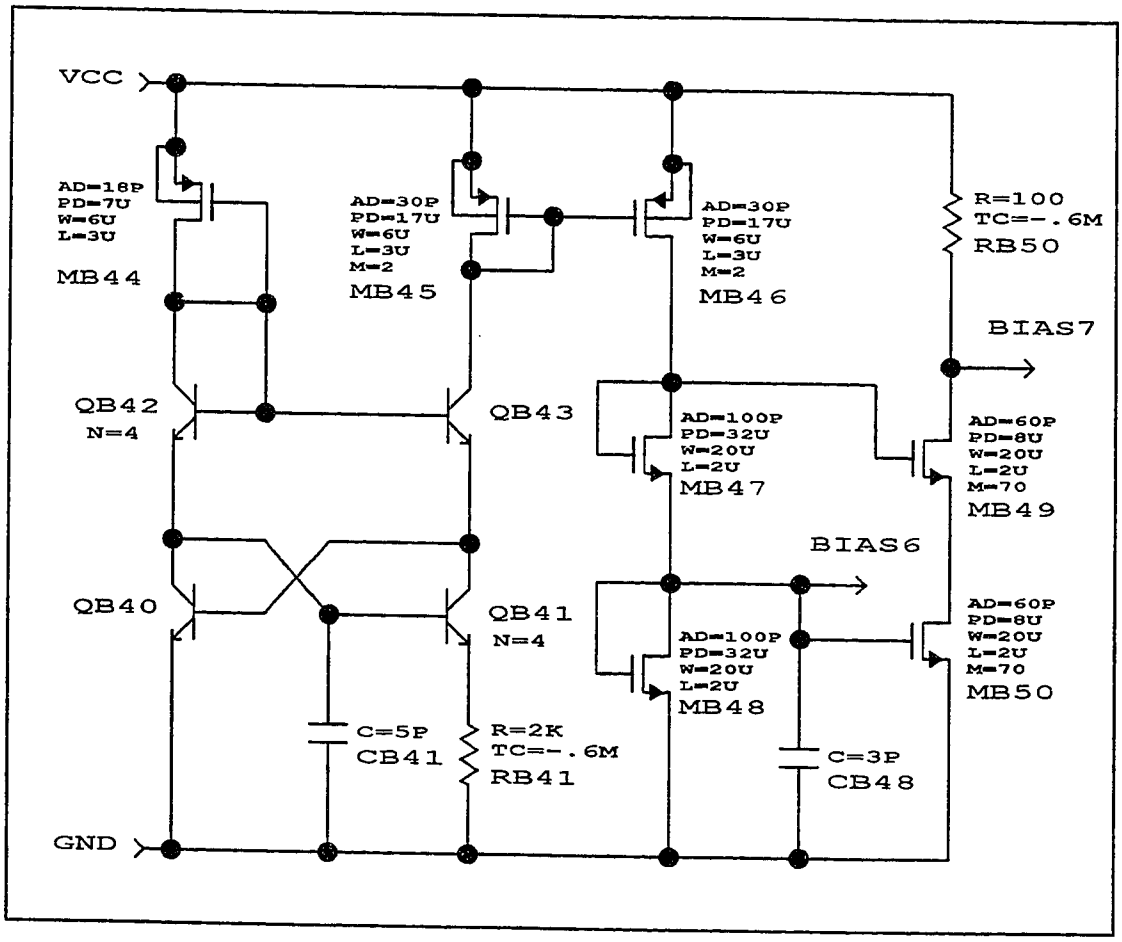

Fig. 16. Comparator Biasing Circuit

A Delta-V_{be} cell using a translinear cross-quad [49], shown in fig. 16, performs this function. The reference current is set by the voltage across R_{B41}, which is set by a ratio of transistor's emitter areas:

$$V_{BE42} + V_{BE41} + I_{RB41} R_{41} = V_{BE43} + V_{BE40}$$

$$V_T \ln \frac{I_{42}}{4\, I_S} + V_T \ln \frac{I_{41}}{4\, I_S} + I_{RB41} R_{B41} = V_T \ln \frac{I_{ref}}{I_S} + V_T \ln \frac{I_{40}}{I_S}$$

$$I_{RB41} = \frac{(\beta+1)}{\beta} I_{41}$$

$$\frac{(\beta+1)}{\beta} I_{Ref} = I_{41} + \frac{I_{40}}{\beta}$$

$$I_{42} = \frac{I_{41}}{\beta} + I_{40}$$

Combining the previous equations and defining $X = \frac{I_{42}}{I_{ref}}$:

$$I_{Ref} = \frac{V_T}{R_{B41}} \frac{(\beta^2-1)}{(\beta+1)(\beta+1-X)} \times \ln\left[\frac{16\beta}{(\beta+1)} \frac{\left(1-\frac{(\beta+1)}{\beta^2 X}\right)}{\left(1-\frac{X}{(\beta+1)}\right)}\right]$$

$$I_{Ref}(\beta\to\infty) = \frac{V_T}{R_{B41}} \times \ln(16)$$

$$\frac{I_{Ref}}{I_{Ref}(\beta\to\infty)} = \frac{(\beta^2-1)}{(\beta+1)(\beta+1-X)\ln(16)} \times \ln\left[\frac{16\beta}{(\beta+1)} \frac{\left(1-\frac{(\beta+1)}{\beta^2 X}\right)}{\left(1-\frac{X}{(\beta+1)}\right)}\right]$$

For a process with ß between 50 and 150, the reference current is closest to the ß=∞ case for $I_{42} \cong 2I_{Ref}$. If I_{42} varies between I_{Ref} and $3I_{Ref}$, and ß=50, the reference current varies ±3%, and the variation is smaller as ß increases.

I_{42} is not only process and temperature dependent but also power supply dependent, since most of the power supply variations are directly applied between the source and gate of M_{B44}.

By making the reference resistor and the amplifier's load resistors equal, and by making the transistor's bias

currents three times the reference current, then the gain of the emitter coupled pair is:

$$\frac{V_{5-6}}{V_{1-2}} = -3 \ln 16 \cong -8.3,$$

independently of resistance and absolute temperature.

The cross-quad circuit of fig. 16 has positive and negative feedback loops. The circuit is compensated with a 5pF capacitor C_{B41} so that the positive feedback loop is always slower than the negative feedback loop.

A reference voltage, 300mV under the power supply, to set the common mode voltage at the gates of MA1 and MA2, is obtained by forcing a constant current through R_{B50}.

The value of the common mode reference is not arbitrary. It has to be sufficiently low so that the parasitic diodes between the drain and substrate of MI1 and MI2, do not turn-on during the switching transients before the comparison takes place (fig. 13). If the parasitic diodes were turned-on, the information stored at the sampling capacitors would be lost. For the same reason the n-well is connected to the highest possible voltage (V_{cc}).

Nodes N10 and N11 can be pre-charged to V_{cc} because their swing is restricted to ±216mV by nodes N5 and N6. And this swing does not cause any problem.

With respect to the frequency response at the bases and collectors of QA5 and QA6, it can be seen that in both cases the time constants can be reduced by increasing the current.

At node N1 increasing the current increases gm_1 proportionally, and at node N3 increasing the current allows to decrease R_{A5} proportionally, due to the constraint Ic R_{A5} = constant. Considering this constraint, as well as the fulfillment of the timing requirements, while maintaining the power dissipation as low as possible, the following values are used: $R_{A5} = R_{A6} = 2K\Omega$, $I_5 = I_6 = 108\mu A$.

The worst case settling for this amplifier, is when the input goes from the maximum difference in one direction to the minimum difference in the other direction. As an example consider a step input from V_{id} = -1V to V_{id} = +2mV. The output is consequently forced from V_{N9-N8} = -216mV to $V_{N11-N10}$ = 9.6mV. However, for proper operation it is enough to reach 5mV; therefore, 3.9 times constants ($e^{-n} = \frac{9.6-5}{216+9.6}$, or n = 3.9), are needed to settle to the required precision. And since the settling time should be smaller than 12ns, the addition of the time constants should be smaller than 12ns/3.9, or 3.1ns.

At N8 or N9 with a 72μA current through QA8 or QA9, the time constant is calcullated as follows:

$$C_{N8/N9} = \frac{C_{of}\, C_{inlatch}}{C_{of} + C_{inlatch}} + C_{\pi 8} + C_{OL10} + C_{BD10} = 700fF$$

$$\tau_{N8/N9} = \frac{C_{N8/N9}}{g_{m8/9}} = .25ns$$

At N5 or N6:

$$C_{N5/N6} = C_{\mu 5} + C_{CS5} + C_{\mu 8} + C_{\pi 8} = 610fF$$

$$\tau_{N5/N6} = R_{A5/A6}\, C_{N5/N6} = 1.22ns$$

At N1 or N2 with a 216μA current through MA1 and MA2:

$$C_{N1/N2} = C_{\mu 5}\,(1-A_{5/6}) + C_{\pi 5} + C_{DB3} + C_{SB1} + C_{OL}\,(W1+W3) + \frac{2}{3}\,C_{ox}\,W1\,L1 = 1.2pF$$

$$R_{N1/N2} = \frac{1}{g_{m1} + g_{mb1}} = 812\Omega$$

$$\tau_{N1/N2} = .95ns$$

Therefore the overall time constant during the comparison is

$$\tau = 2.42ns$$

In reset mode, the load at N8 of N9 is C_{of} instead of about $C_{of}/4$, and the overall time constant becomes 2.9ns. And considering that 24ns, or 8.3 time constants are assigned to the reset operation, an initial differential voltage of 432mV settles to about .1mV $432mV\,e^{-8.3} = .1mV$, which is satisfactory for this application.

3.3 *Regenerative Latch Design*

The latching process is done in two steps. In the first one, the output of the comparator's amplifier is further amplified by a bipolar latch, and in the second one, it is transferred to a MOS latch that completes the operation by taking the outputs to adequate logic levels [50]. Fig. 17 and fig. 18 show the complete latch. Nodes N10 and N11 are the same shown in fig. 15.

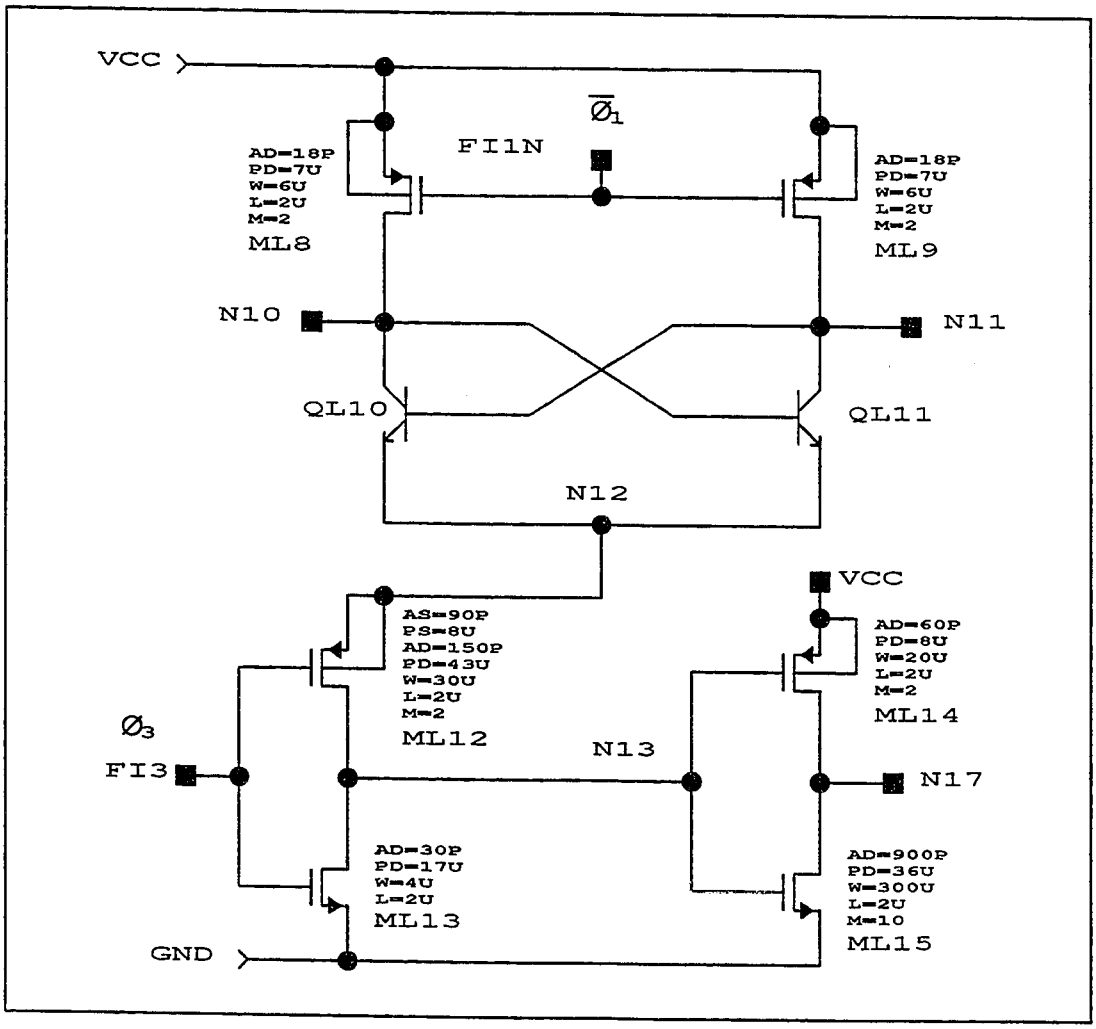

Fig. 17. Bipolar Latch

During the reset mode, $\overline{\Phi_1}$ is low and ϕ_3 is high. Nodes N10 and N11 are charged to V_{cc}, nodes N22 and N23 are reset to ground, and the timing capacitance at node N13 is discharged. Node N13 low keeps node N17 high and ML20 and ML21 turned off. Therefore the CMOS latch, formed by ML22 and ML23, is isolated from nodes N10 and N11.

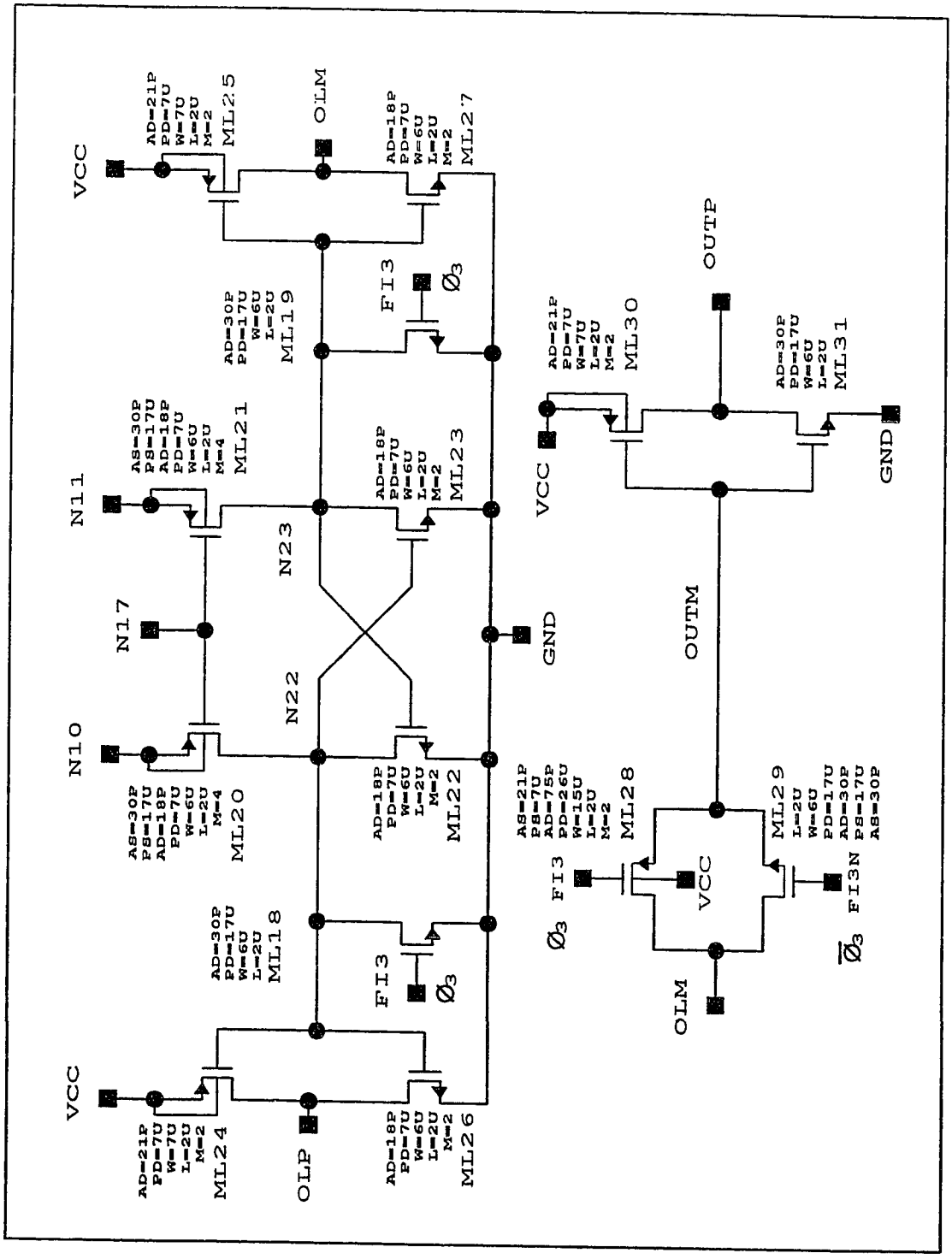

Fig. 18. CMOS Latch

When $\overline{\Phi_1}$ goes high the offset of the amplifier is sampled on C_{of}. From this moment there is no current path from nodes N10 and N11, and the charge is conserved. Then, the amplified version of the difference between the reference and the input signal is developed as $V_{N10-N11}$. When $V_{N10-N11}$ is big enough to be resolved by the bipolar latch, formed by QL10 and QL11, ϕ_3 goes to low, turning on ML12. The charge at nodes N10 and N11 has now to be shared with the capacitance at N13 through the bipolar transistors. $V_{N10-N11}$ is also a difference in the V_{BE} of QL10 and QL11, and it is regeneratively increased as N13 is being charged, due to the positive feedback of the cross-coupled transistor configuration. All the charge that is pumped to N13 comes from the C_{of}^{+} and C_{of}^{-}, therefore, V_{N13} is related to $V_{N10-N11}$ as:

$$V_{N13} = \frac{2\,C_{of}}{C_{N13}}\,V_{N10-N11}$$

The CMOS latch is triggered when V_{N13} exceeds the threshold voltage of the inverter, connected between nodes N17 and N13. It is a requirement that $V_{N10-N11}$ be more than the expected offset from the CMOS latch, before it can be triggered. This condition is guaranteed by adjusting C_{N13}, according to the previous equation.

When ML20 and ML21 are turned on, $V_{N10-N11}$ is coupled to nodes N22 and N23, and subsequently increased to CMOS levels. Once OUTP and OUTM have reach the final values, the

transmission gate formed by ML28 and ML29 is closed and the comparator is reset.

CHAPTER 4

Track-and-Hold Operational Amplifier Design

The inclusion of a track-and-hold amplifier plus sampling capacitors enhances the converter's performance by isolating the comparator's inputs from analog signal variations while the comparisons are taking place. At the same time, the high input impedance amplifier significantly reduces the loading of the analog signal source.

This chapter covers the amplifier design. From the external constraints, the amplifier specifications are derived. Then an appropriate circuit configuration is designed.

4.1 *Amplifier Specifications*

The track-and-hold amplifier is a fully differential operational amplifier connected in unity gain configuration. The analog signal source is expected to provide a ±1V maximum differential swing. The output has to settle in 24ns to a LSB/4 of accuracy following an input differential step of 2V. The loading is determined by the parallel combination of the sampling capacitors plus the parasitics

due to the amplifier itself. The total is 44pF at each single ended output.

The dc open loop gain of the amplifier (A), is determined from the accuracy specification, and from the maximum swing. The output voltage of an operational amplifier connected in unity gain configuration is very close but not exactly equal to the input voltage:

$$V_{od} = \frac{A}{A+1} V_{id}$$

Therefore the relative error is:

$$\frac{V_\varepsilon}{V_{id}} = \frac{V_{id} - V_{od}}{V_{id}} = \frac{1}{A+1}$$

And considering that the maximum absolute error will occur for the maximum V_{id}:

$$\frac{1}{A+1} \leq \frac{LSB/4}{2^8\ LSB}$$

$$A \geq 1023 \ (60.2\text{dB})$$

The settling time has a slewing component and a linear component. The first one is limited by the capacitance and available current at the nodes that experience large swings. The second component is limited by the amplifier's bandwidth. The smaller the slewing period, the larger the current and the power consumption. The smaller the linear settling period, the higher the bandwidth requirements. As a trade-off between the two, 9ns are allotted for slewing and 15ns for linear settling.

The maximum step ΔV that each output can experience is 1V, and it can be assumed that the slewing is dominant during 90% of it, therefore the minimum slew rate should be:

$$Slew\ Rate = \frac{\Delta V}{\Delta t} = \frac{I}{C}$$

$$SlewRate \geq \frac{0.9\ \Delta V_{MAX}}{\Delta t} = \frac{0.9\ 1V}{9ns} \cong 100\frac{MV}{s}$$

The linear settling initial value is a 10% of the original step, and n time constants are needed to achieve a precision of a LSB/4 (2mV differential or 1mV single ended), where

$$n \geq -\ln\left(\frac{1mV}{0.1\ 1V}\right) = 4.6$$

The time constant is:

$$\tau \leq \frac{15ns}{n} \leq 3.26ns$$

And the open-loop unity gain bandwidth of the amplifier is:

$$f_u \geq \frac{1}{2\pi\tau} \geq 49MHz$$

4.2 *Output Stage*

Due to the unity gain configuration, the input and output swings are equal. An NPN class A output stage is utilized because of its driving capabilities, good frequency response, and simplicity. Fig. 19a shows that the swing is restricted down to a V_{DSsat} from ground, and up to V_{DSsat} plus V_{BE} from the supply voltage. Fig. 19, parts b, c, and d, show three options for the input stage. The only one that can be practically used with a 3V power supply and the

output stage of fig. 19a is the PMOS differential pair. If an NPN or NMOS differential pair were used, the minimum input voltage to keep the NMOS current source in saturation is V_{BE} plus V_{DSsat}, or V_{gs} plus V_{DSsat} respectively. In both cases the total swing would be less than the requires 1V peak.

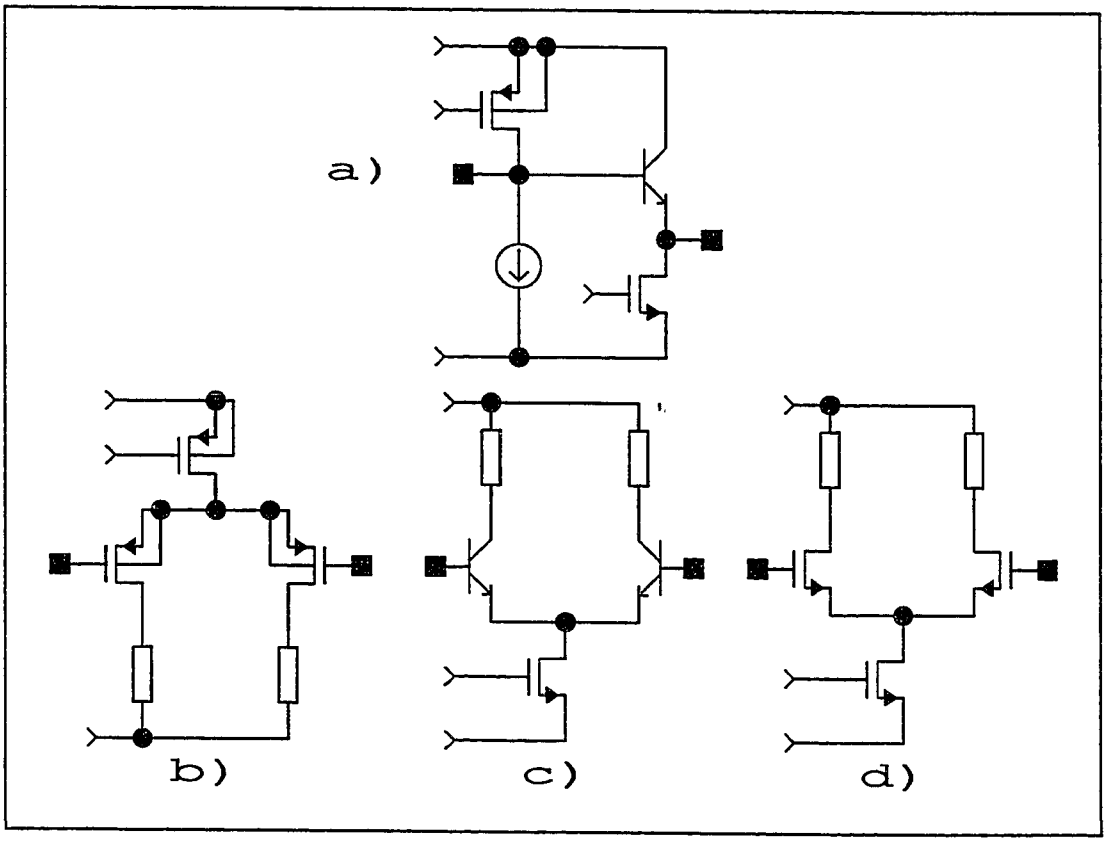

Figure 19. Input and Output Common Mode Swing. a) Class A, NPN Output Stage; b) PMOS Differential Pair; c) NPN Differential Pair; d) NMOS Differential Pair

The output current should be enough to satisfy the timing constraints of section 4.1.

The maximum ΔV at each output is 1V, and assuming that the slewing is dominant during 90% of it, the necessary current is calculated as follows:

$$I_{slew} \geq C \times S.R. = 55pF\ 100\frac{MV}{S} \cong 5.5mA$$

The pole given by the output capacitance and the NPN output driver, $\frac{g_{mout}}{C_{out}}$, should be several times larger than the amplifier's unity gain frequency to keep its phase shift contribution small. This condition has to be maintained even when the output is slewing. Therefore, the bias current has to be larger than the calculated for slewing requirements, so that the pole is still high in worst case conditions.

The additional current is calculated setting the pole at ten times f_u:

$$\frac{g_m}{C_{out}} = \frac{I_{pole}}{V_T C_{out}} = 10 \times 2\pi f_u$$

$$I_{pole} \cong 4.5mA$$

And the total output current is:

$$I_{out} \geq I_{slew} + I_{pole} \cong 10mA$$

It is noted that the actual pole is at five instead of ten times the unity gain frequency due to transconductance degradation described later in this chapter.

4.3 *Amplifier*

The main amplifier consist of a BiCMOS folded cascode stage where the substitution of common gate MOSFETs for common base BJTs significantly improves the frequency response (fig. 20). For the amplifier to be fully differential and to be connected in unity gain configuration, two input source coupled pairs are required. The differential voltage at the input to each of the pairs is converted to current and then subtracted. Then, the difference between the currents is converted back to voltage at the amplifier output nodes (OAP and OAM).

For sufficiently high input voltage, a current of two times I_{M1} is added to I_{M11} and subtracted from I_{M12} or viceversa. To avoid turning off either transistor, the bias current through M11 and M12 should be somewhat higher than twice the bias current of the input transistors.

The dc voltage gain is the transconductance of the input transistors times the resistance at either OAP or OAM. One design equation is obtained assuming that the dominant resistive factor at nodes OAP and OAM is the output resistance of transistors M11 and M12, and noting reminding that the gain should be greater than 60.2dB:

$$g_{m1}\, r_{o11} \geq 511$$

$$\sqrt{2\, KP_{M1}\left(\frac{W}{L_{eff}}\right)_{M1} I_{M1}} \times \frac{L_{effM11}}{\lambda_p 1.5\mu m\, I_{M11}} \geq 1023$$

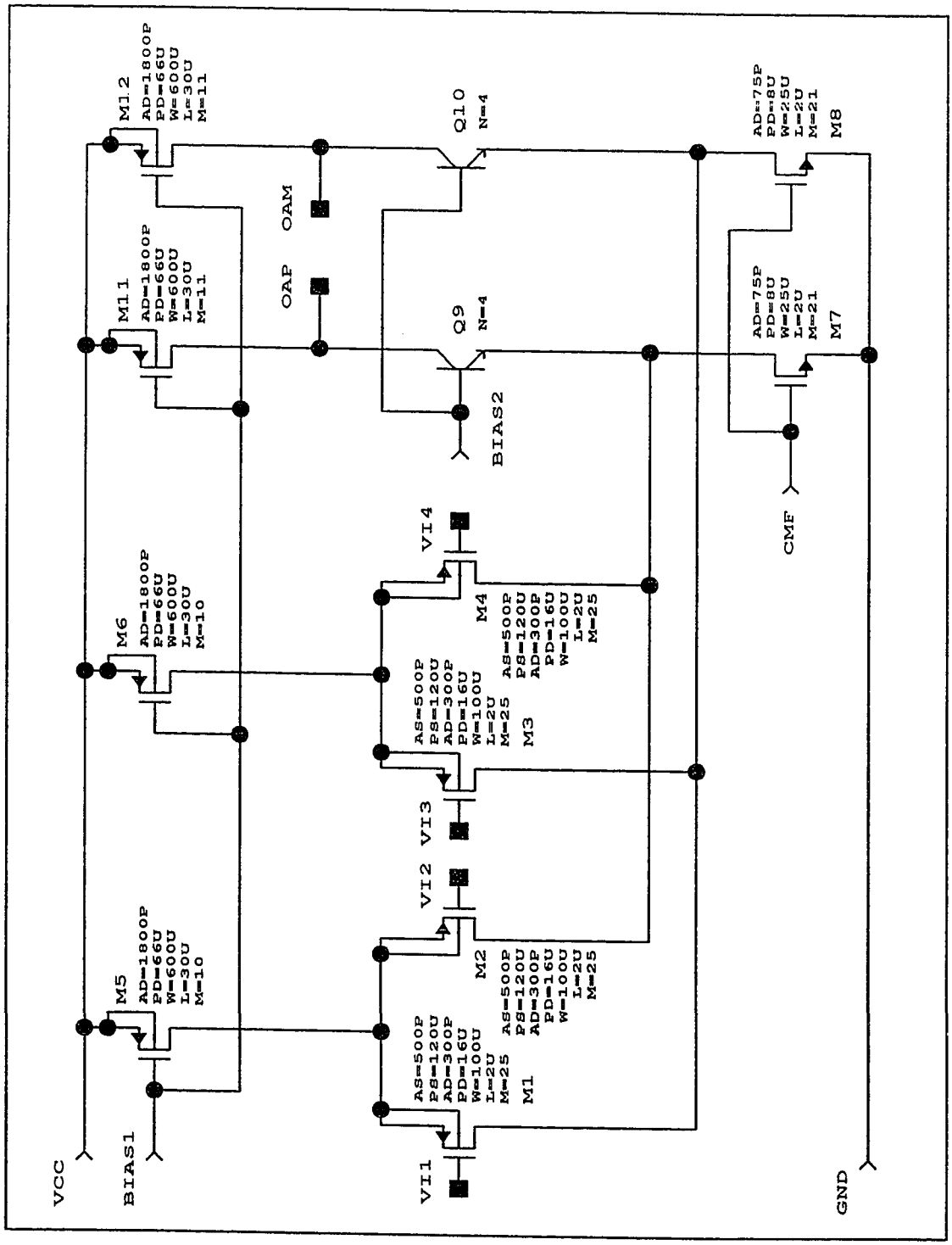

Figure 20. Differential Folded Cascoded Amplifier

$$1.6\frac{nA}{\mu m^2} L_{effM11}^2 \left(\frac{W}{L_{eff}}\right)_{M1} \geq I_{M1} \qquad (1)$$

A second design equation is obtained from the requirement that the unity gain bandwidth of the amplifier has to be greater than 50MHz, and it is the transconductance of the input transistors divided by the capacitance at either OAP or OAM.

$$\frac{g_{mM1}}{C_{OA}} \geq 2\pi\, 50MHz$$

$$\left(\frac{W}{L_{eff}}\right)_{M1} I_{M1} \geq 2.15\frac{mA}{pF^2} C_{OA}^2 \qquad (2)$$

From the slewing specification, and choosing the bias current at M11 and M12 as 10% larger than twice I_{M1}:

$$\frac{2.2\, I_{M1}}{C_{OA}} \geq SlewRate_{\min}$$

$$I_{M1} \geq 45\frac{\mu A}{pF} C_{OA} \qquad (3)$$

The overdrive voltage of transistors M11 and M12 should be small so that their output resistance is not significantly degraded by driving the transistors very close to triode operation. Nodes OAP and OAM swings between 1.1V and 2.1V. In the extreme case of a 3V power supply, V_{SDM11} can be as low as 900mV. Allowing 300mV margin from the limit of saturation, and considering the 300mV threshold voltage, $|V_{gsM11} - V_{tM11}|$ should be less than 600mV. Therefore,

$$\left(\frac{W}{L_{eff}}\right)_{M11} \geq \frac{I_{M1}}{1.9\mu A} \qquad (4)$$

Regarding C_{OA}, it has a contribution of about 1pF from the following stage and about 300fF for each transistor connected as Q9 or Q10, and one transistor is used for every 300uA. But the largest component is from M11 or M12 and it is about $.9\frac{fF}{\mu m} \times W_{M11}$. Adding the three terms,

$$C_{OA} \cong 1pF + 2.2\frac{fF}{\mu A} I_{M1} + .9\frac{fF}{\mu m} W_{M11} \qquad (5)$$

The design of the amplifier is done adjusting equations (1) to (5) to allow for process and temperature variations, and then iterating until appropriate current and transistor sizes are obtained.

4.4 *Buffer Stage*

In order for the amplifier to have a high gain, the resistance of its loads must also be high. In the order of hundreds of KΩs. And since the input resistance of the output stage is a few KΩs, an intermediate buffer stage is added.

Fig. 21 shows the buffer and output stages. Source followers M13 and M14 provide an extremely high input resistance, diodes Q17 and Q18 act as level shifters, Q21 and Q22 are the output drivers, and the remaining transistors are current sources.

In section 4.1 the output current was calculated to keep the output pole ten times larger than the unity gain frequency. Under low current conditions those calculations

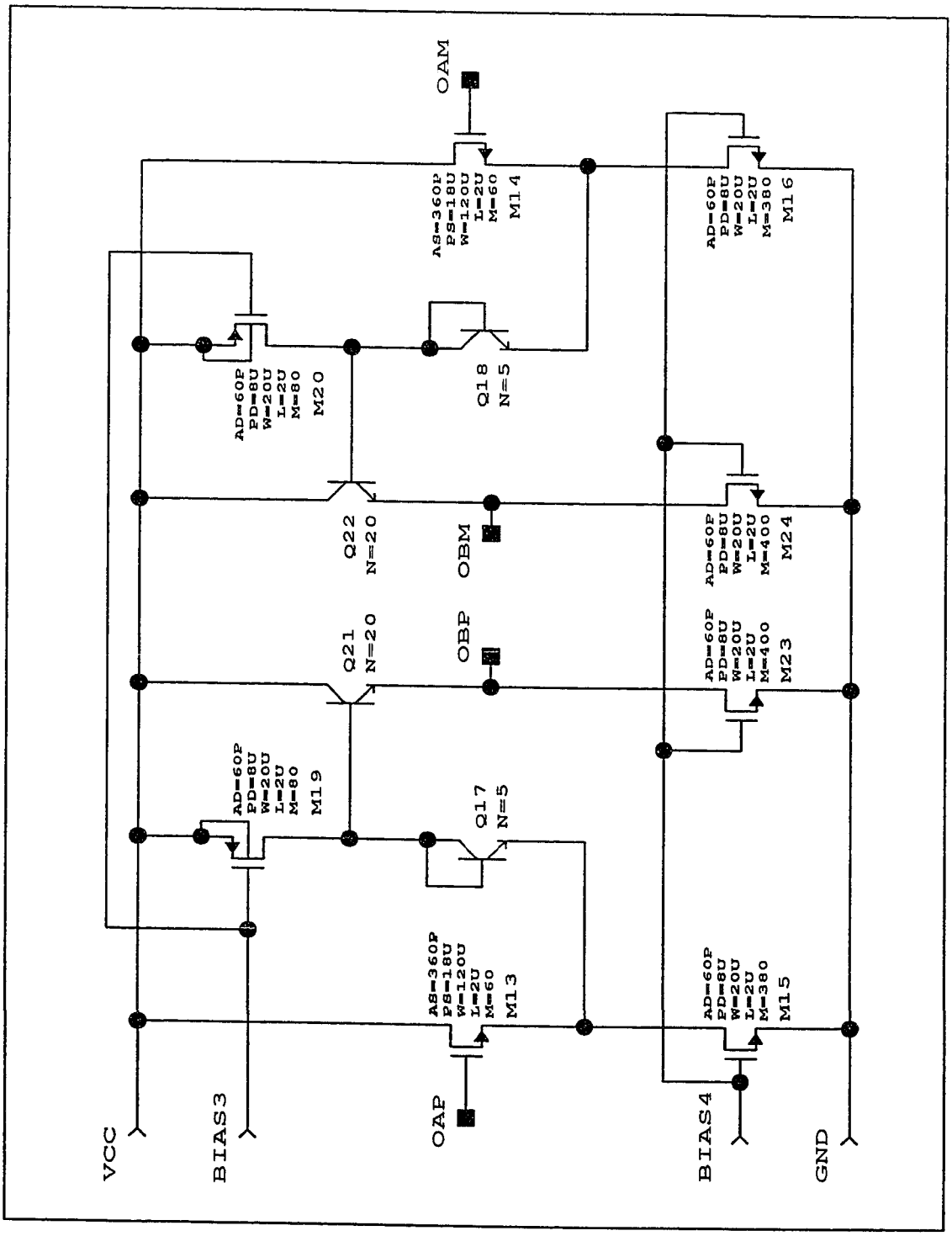

Figure 21. Intermediate Buffer Stage

are accurate, but when the current is of several milliamps, the g_m is degraded by the emitter and base resistances, and by the resistance seen from the bases of Q21 or Q22.

$$\frac{1}{g_{meff}} = \frac{1}{g_{m21}} + r_{e21} + \frac{1}{\beta_{21}}\left(r_{b21} + \frac{1}{g_{m17}} + r_{e17} + r_{b17} + \frac{1}{g_{m13}}\right)$$

With the values chosen in this design, the output pole is five times larger than the open loop unity gain frequency of the amplifier.

4.5 *Common Mode Feedback Circuit*

The common mode feedback amplifier of fig. ? senses the common mode output voltage, compares it with a reference of 1V, and adjusts the current at the amplifier accordingly through M7 and M8. The sizes of the transistors are chosen so that the open loop gain of the common mode feedback circuit is somewhat lower than that of the main loop. In this way, both loops are compensated together, both loops have the similar bandwidth, and the circuit is not slowed down by the common mode feedback loop.

The sensing resistors between nodes OBP and OBM should not load the output of the operational amplifier. At the same time they should be small to neglect the pole at the gate of M25.

The current through the common mode feedback amplifier is chosen high enough for the pole at the drain of M26 to be also very high.

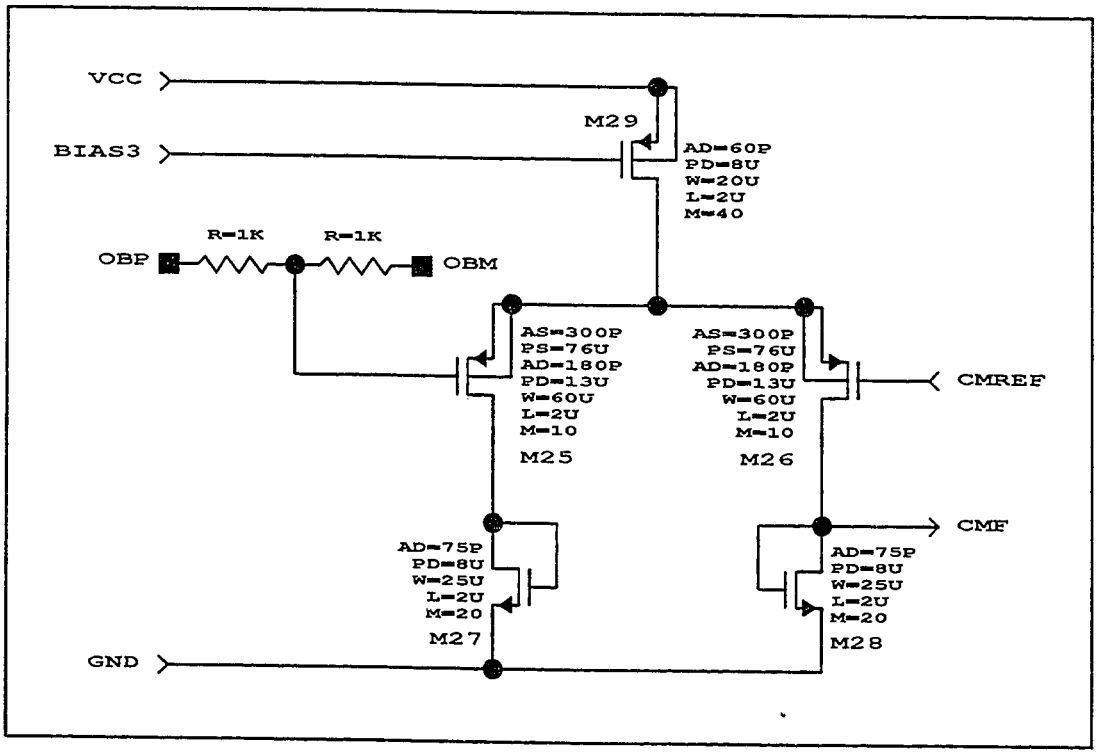

Figure 22. Common Mode Feedback Amplifier

4.6 *Operational Amplifier Bias Circuit*

The bias circuit shown in fig. 23 [51], sets the operating point as the intersection of two I-V characteristic curves. The one given by M36 and M37 is quadratic, while the other given by Q30, Q31, M32, and M33 is exponential.

The current is calculated noting that the mirrored transistors M36 and M37 force the current to be equal on both sides of the bias cell, and writing the following equation:

$$V_{BE30} + V_{sg32} = V_{BE31} + V_{sg33}$$

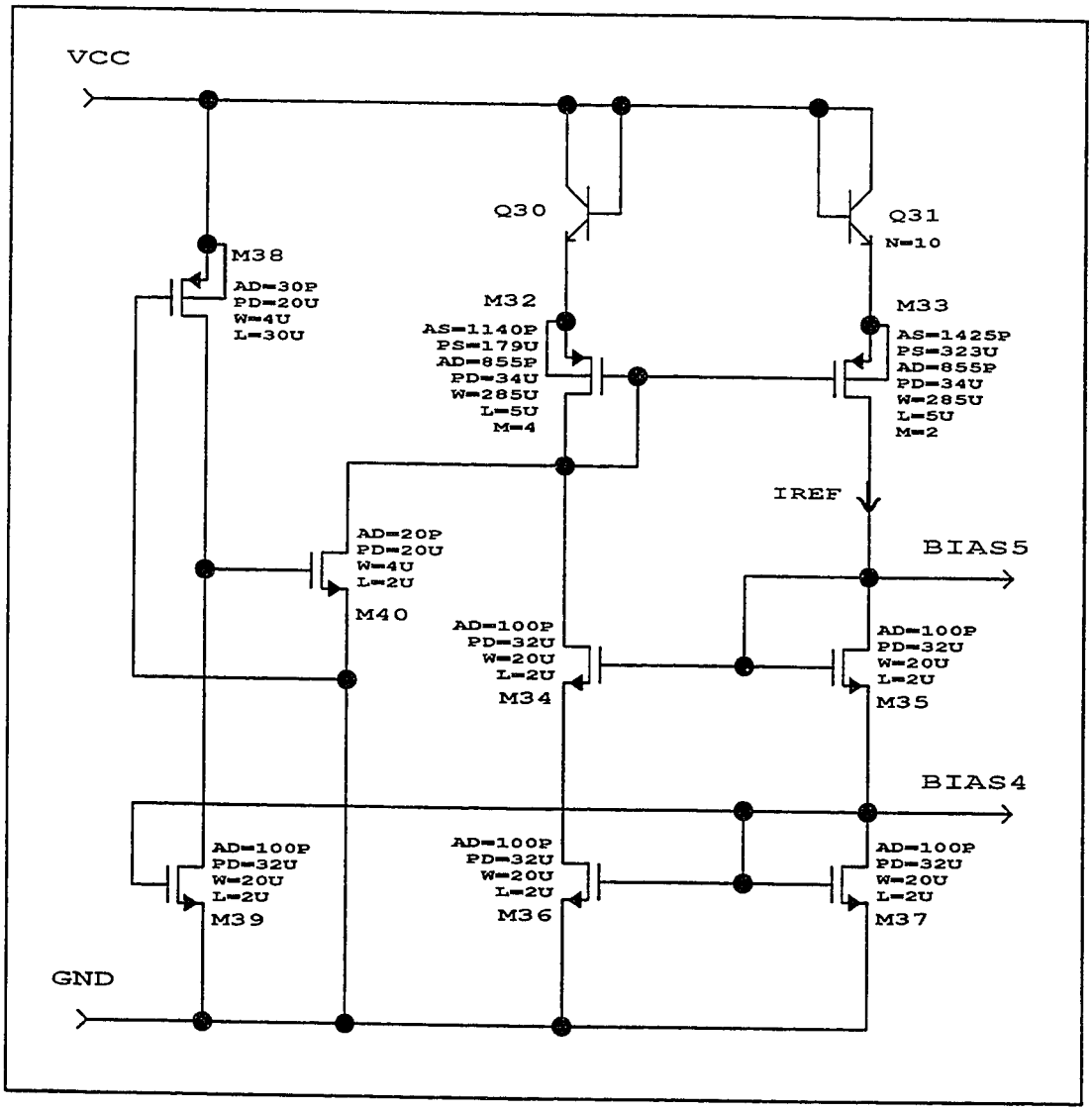

Figure 23. Reference Circuit

$$V_T \ln\left(\frac{I_{ref}}{I_{S30}}\right) + V_{th} + \sqrt{\frac{2\,I_{ref}}{KP_p\left(\frac{W}{L_{eff}}\right)_{32}}} = V_T \ln\left(\frac{I_{ref}}{I_{S31}}\right) + V_{th} + \sqrt{\frac{2\,I_{ref}}{KP_p\left(\frac{W}{L_{eff}}\right)_{33}}}$$

And if $I_{S31} = K1\ I_{S30}$ and $\left(\frac{W}{L_{eff}}\right)_{32} = K2\left(\frac{W}{L_{eff}}\right)_{33}$

Then, $$I_{ref} = \frac{KP_p}{2}\left(\frac{W}{L_{eff}}\right)_{33}\left(\frac{V_T \ln K1}{1 - K2^{-\frac{1}{2}}}\right)^2$$

A very attractive characteristic that follows from this result is that the current is proportional to only the square root of the absolute temperature:

$$V_T \propto T \quad \text{and} \quad KP \propto T^{-\frac{3}{2}}$$

$$\therefore \quad I_{ref} \propto T^{\frac{1}{2}}$$

At the beginning of this section it was said that the operating point is the intersection of a quadratic and an exponential characteristic. The two curves crosses each other not only at the desired bias point but also at the origin given a second stable point with no current at all.

To prevent the circuit from staying at a non-current state, a start-up circuit is added. The idea of the circuit is to detect the undesired state and to force the bias cell into the desired state by pulling down the gates of transistors M32 and M33. After reaching the desired operating point the start-up circuit should disconnect itself to avoid affecting the normal operation of the main cell. Looking at fig. 23, it can be seen that M38 is always on, and trying to keep M40 also on. If the circuit is in a zero current state, M40 pulls the gates of M32 and M33 down, forcing some current through the cell, and therefore turning-on transistors M36, M37, and M39. Once M39 is on,

the high ratio between the output impedances of M38 and M39 keeps the voltage at the gate of M40 close to zero, and transistor M40 off.

All the references required in the different parts of the circuit are generated from the main reference as shown in fig. 24. BIAS1, BIAS3, and BIAS4 are used to bias current sources. BIAS2 sets the voltage at the bases of Q9 and Q10 (fig. 20). CMREF is the voltage reference for the common mode feedback amplifier (fig. 22). It is determined by a reference current through a diode connected NMOS and another NMOS operating in triode region. Writing the transistor equations, and noting that both transistors have the same size:

$$CMREF \cong V_{th} + \sqrt{\frac{4\ I_{M50}}{KP_n\left(\frac{W}{L_{eff}}\right)_{M51/M52}}}$$

BIAS2 is obtained with a V_{BE} multiplier and it is 1.7 times V_{BEQ45}.

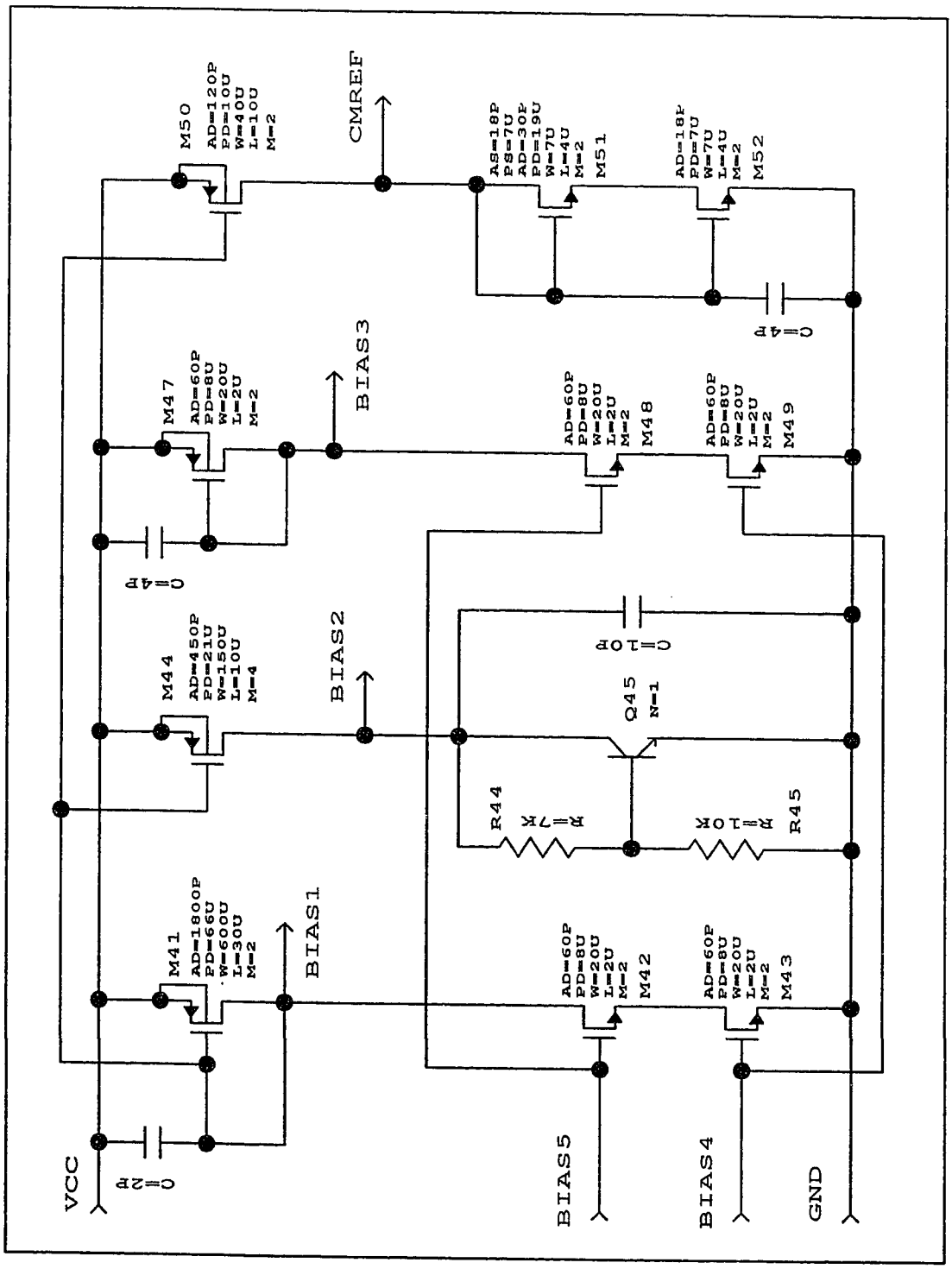

Figure 24. Bias Generation from Main Reference

CHAPTER 5

Decoder and Phase Generation

5.1 *Decoder*

The result of each coversion of the flash A/D converter is a 255-bit word in thermometer code. The bits corresponding to comparators whose references are lower than the value of the sampled analog signal are 'ones'; the others are 'zeros'.

This word is translated to a 'One in N' code word, where all digits but one are 'zeros'. The one indicates the comparator with highest reference voltage whose output is a 'one'.

Finally, the 'One in N' code word addresses a 255 x 8 ROM whose output is the 8-bit version of the sampled analog signal.

The translation to 'One in N' is implemented with a set of 255 3-input NAND gates configured to detect a sequence of two 'ones' followed by a 'zero' at the thermometer code word. The use of 3 instead of 2-input gates adds a simple error correction algorithm to the circuit.

An error occurs if the result of a comparison is incorrect. If the error corresponds to a bit next to the transition point, the result is one LSB away from the

correct result. If the error is in any other bit and 2-input gates are used to detect a 'one-zero' transition, the problem is more important because two bytes of the ROM are addressed at the same time and the two bytes are wired OR. For this last kind of error to occur in a 3-input gate implementation, the result of the comparisons should have two sequences 110, which is much less probable.

Fig. 25 shows the implementation of a 3-bit example.

5.2 *Clock Phases*

The clock phases required on-chip are internally derived from an external clock that sets the conversion rate. The circuit used for the generation of each clock phase is based on the block diagram of fig. 26.

At the diagram, ϕ_0 is the master clock while ϕ_1 and ϕ_2 are the derived clock phases. There are two possible steady-states: One in which ϕ_0, ϕ_1, and ϕ_2 are 0, 0, and 1 respectively, and the opposite in which they are 1, 1, and 0.

ϕ_1's rising and falling edges are delayed from ϕ_0's rising and falling edges by A+D+B+C and B+C respectively.

ϕ_2's falling and rising edges are delayed from ϕ_0's rising and falling edges by A+D+E and B+D+E respectively.

This simple circuit provides enough variables to independently adjust the different clock transitions as

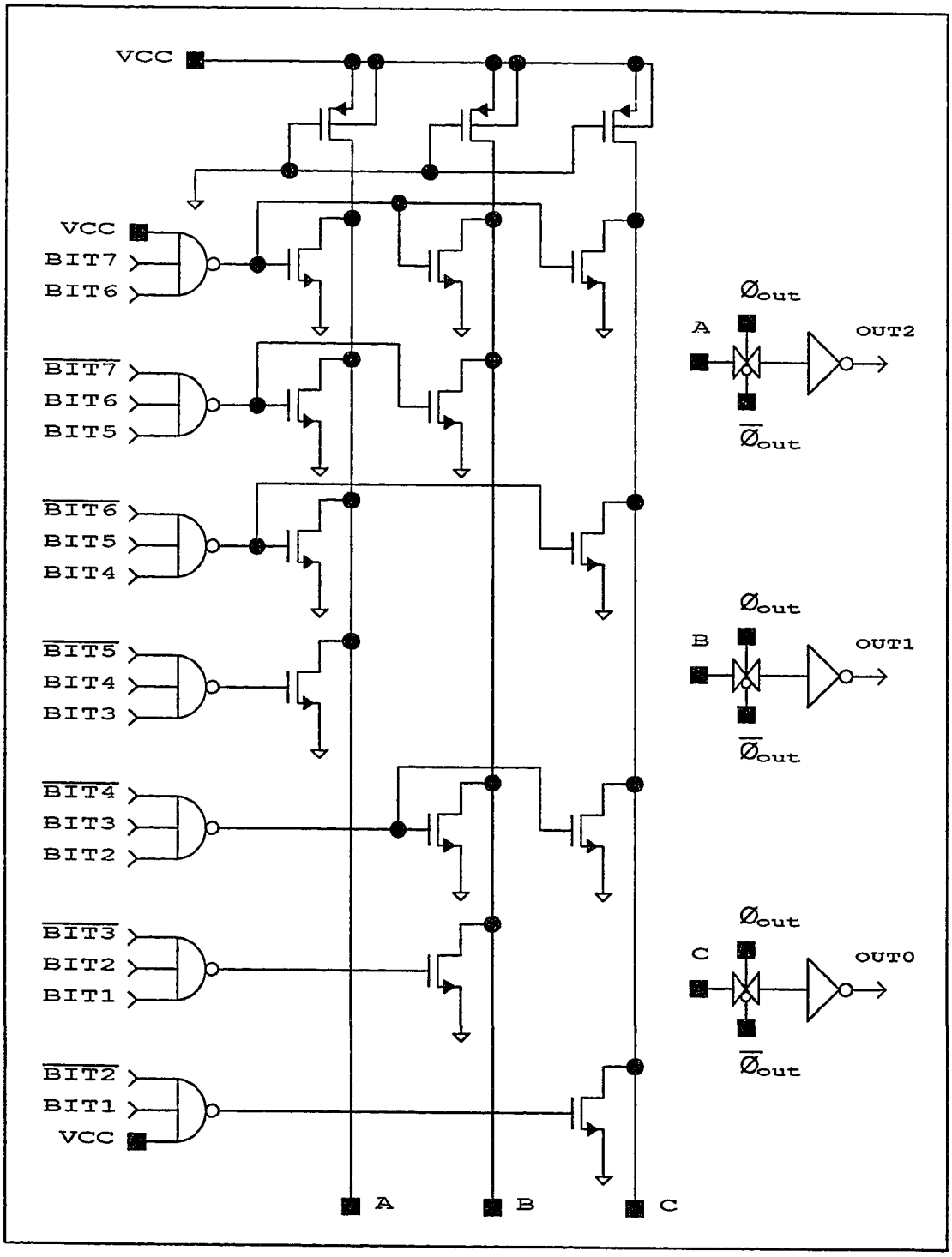

Figure 25. 3-bit Example of Decoder Implementation.

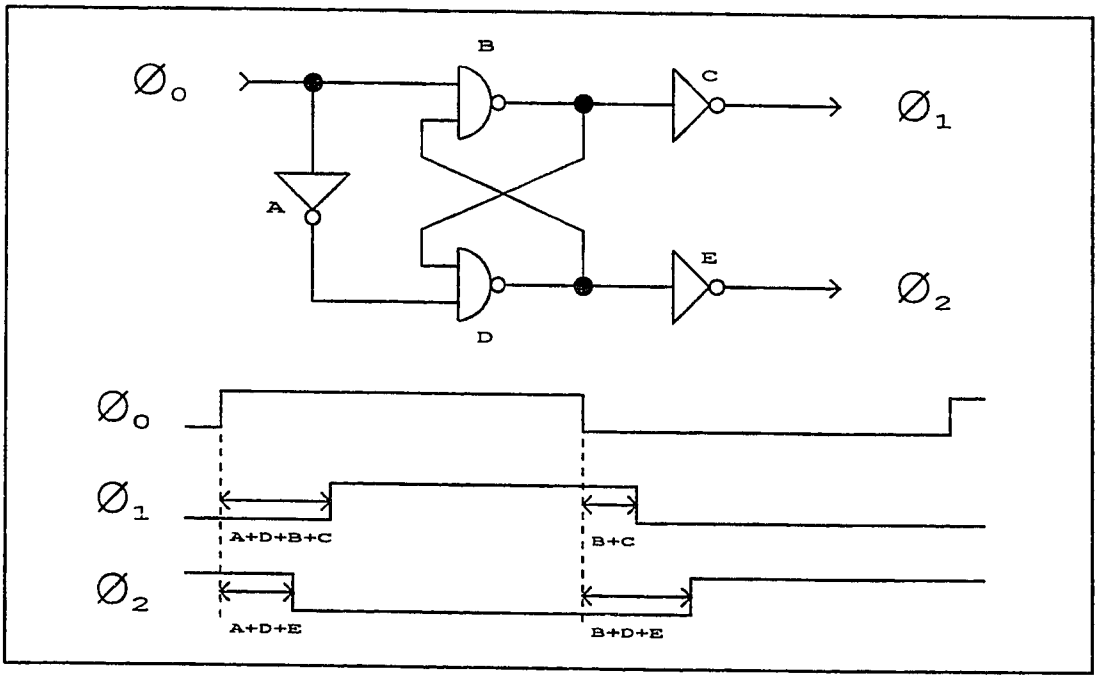

Figure 26. Basic Circuit for Clock Phases Generation

necessary.

CHAPTER 6

Conclusions

One step A/D converters constitute the fastest known architecture, and therefore it is chosen to face a new application that combines video frequencies with low supply voltage.

A fully differential configuration is prefered for both the T/H buffer and the comparators, even if it implies a greater circuit complexity, due to the significant increase in common mode noise and power supply rejection.

The input buffer is a folded cascode BiCMOS amplifier, a source follower, a level shifter, and a class A output stage, all connected in unity gain configuration. The SPICE simulations show a .2% settling time of 24ns. Its frequency response is limited by the phase shift contribution of the second pole of the amplifier and the output stage.

The comparator has an input source follower to provide for the high impedance node required by the sampling scheme. The amplifier stage is a bipolar differential pair whose gain is process and temperature independent.

The latching stage has two parts: a very low offset regenerative bipolat latch followed by a CMOS latch that provides output levels compatible with the following circuitry.

The A/D converter achieves an 18Mb/s conversion rate with an 8-bit resolution and 1LSB linearity.

This research project is an example of the potentiality of BiCMOS technology for modern high speed and low voltage applications. Although the technology used in this project is a modified 2μm CMOS process, the availability of both bipolar and MOS transistors gives a flexibility for circuit topologies that helps on the design of high performance integrated circuits. The combination of a more advance BiCMOS process with multistage architecture is a promising area for further research and will probably constitute a viable solution for low voltage and low power video applications.

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